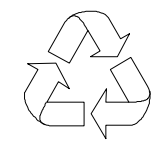
390 Series
Notebook Computer

Service Guide



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Purpose

This service guide aims to furnish technical information to the service engineers and advanced users when upgrading, configuring, or repairing the 390 series notebook computer.

Manual Structure

This service guide contains technical information about the 390 series notebook computer. It consists of three chapters and five appendices.

Chapter 1 System Introduction

This chapter describes the system features and major components. It contains the 390 series notebook computer board layout, block diagrams, cache and memory configurations, power management and mechanical specifications.

Chapter 2 Major Chips Description

This chapter describes the features and functions of the major chipsets used in the system board. It also includes chipset block diagrams, pin diagrams, and pin descriptions.

Chapter 3 BIOS Setup Utility

This chapter describes the parameters in the BIOS Utility screens.

Chapter 4 Disassembly and Unit Replacement

This chapter describes how to disassemble the 390 series notebook computer to make replacements or upgrades.

Appendix A Model Number Definition

This appendix shows the different configuration options for the 390 series notebook computer.

Appendix B Exploded View Diagram

This appendix illustrates the system board and CPU silk screens.

Appendix C Spare Parts List

This appendix lists the spare parts for the 390 series notebook computer with their part numbers and other information.

Appendix D Schematics

This appendix contains the schematic diagrams for the system board.

Appendix E BIOS POST Checkpoints

This appendix lists and describes the BIOS POST checkpoints.

Conventions

The following are the conventions used in this manual:

`Text entered by user`	Represents text input by the user.
`Screen messages`	Denotes actual messages that appear onscreen.
ALT, ENTER, F8, etc.	Represent the actual keys that you have to press on the keyboard.
	**NOTE** Gives bits and pieces of additional information related to the current topic.
	**WARNING** Alerts you to any damage that might result from doing or not doing specific actions.
	**CAUTION** Gives precautionary measures to avoid possible hardware or software problems.
	**IMPORTANT** Reminds you to do specific actions relevant to the accomplishment of procedures.
	**TIP** Tells how to accomplish a procedure with minimum steps through little shortcuts.

Table of Contents

Chapter 1 System Introduction

Chapter 2 Major Chips Description

Chapter 3 BIOS Setup Utility

Chapter 4 Disassembly and Unit Replacement

Appendices

List of Figures

List of Tables

System Introduction

1.1 Overview

This computer combines high-performance, versatility, power management features and multimedia capabilities with unique style and ergonomic design. This computer was designed with the user in mind. Here are just a few of its many features:

- Performance
  - Intel Pentium® processor with MMX™ technology
  - 64-bit main memory and external (L2) cache memory
  - Large LCD display and PCI local bus video with graphics acceleration
  - Internal CD-ROM drive and external 3.5-inch floppy drive, or internal 3.5-inch floppy drive
  - High-capacity, Enhanced-IDE hard disk
  - Lithium-Ion or Nickel Metal-Hydride battery pack
  - Power management system with light green, standby and hibernation power saving modes
- Multimedia
  - 16-bit high-fidelity stereo audio with 3-D sound
  - Built-in dual speakers
  - Ultra-slim, high-speed CD-ROM drive
- Connectivity
  - High-speed fax/data modem port
  - Fast infrared wireless communication
  - USB (Universal Serial Bus) port
- Human-centric Design and Ergonomics
  - Lightweight and slim
  - Sleek, smooth and stylish design
  - Full-sized keyboard and wide palmrest
  - Ergonomically-centered touchpad pointing device
- Expansion
  - CardBus PC card (formerly PCMCIA) slots (two type II/I or one type III) with ZV (Zoomed Video) port support
  - Port replicator option for one-step connect/disconnect from peripherals
  - User-upgradeable memory and hard disk

1.2 System Board Layout

1.2.1 Mainboard

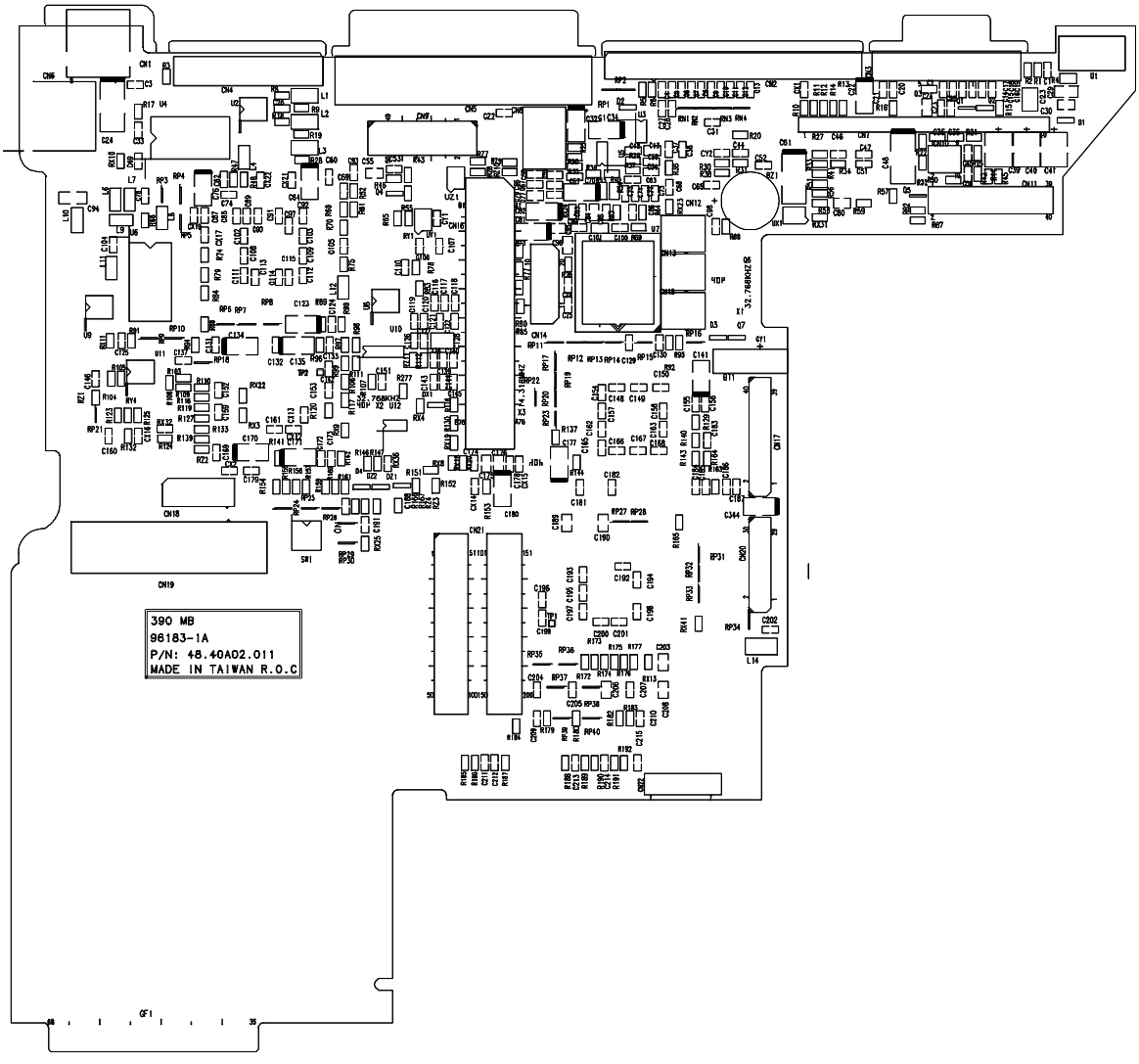


Figure 1-1 PCB No. 96183-1A Mainboard Layout (Top)

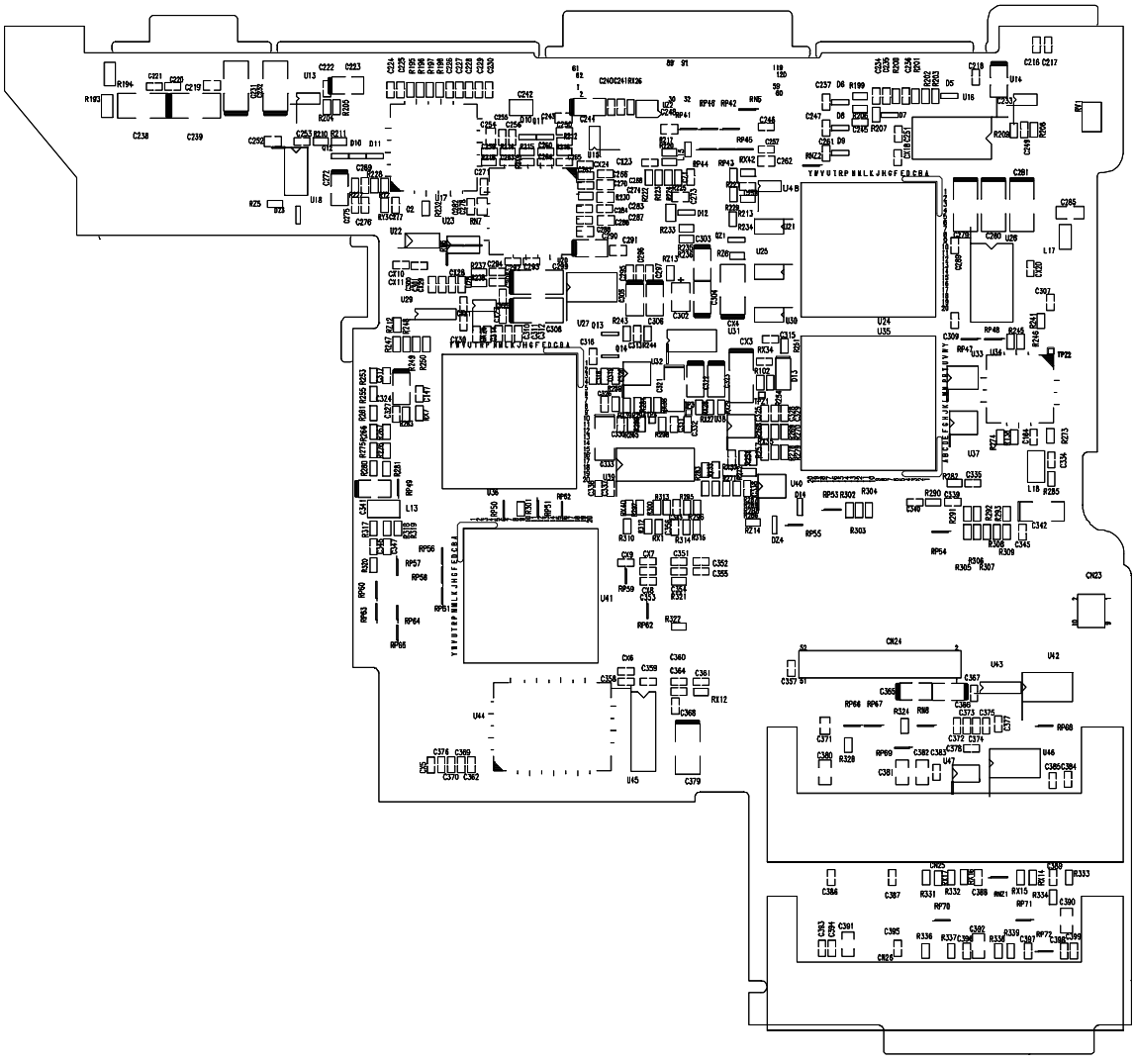


Figure 1-2 PCB No. 96183-1A Mainboard Layout (Bottom)

1.2.2 CPU Board

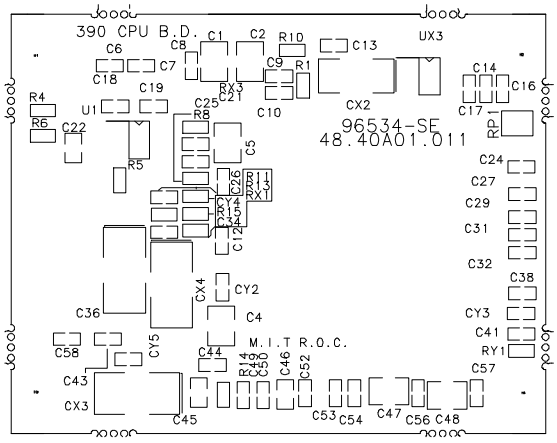


Figure 1-3 PCB No. 96534-SE CPU Board Layout (Top)

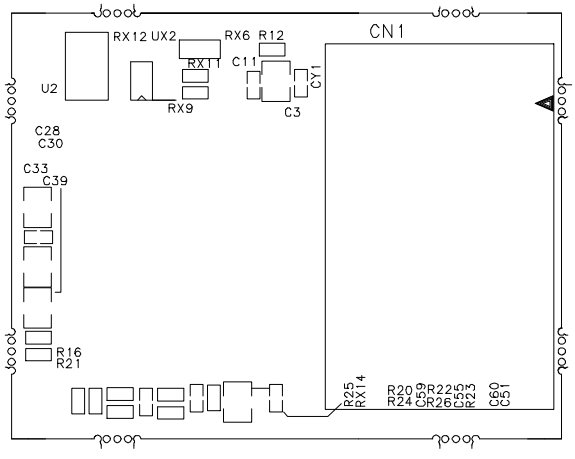


Figure 1-4 PCB No. 96534-SE CPU Board Layout (Bottom)

The following table is a reference when mounting[1] the CPU.

Table 1-1 CPU Mounting Reference Table

			Volt.		Ext Freq		Ratio											
CPU	Volt	Freq	R4	R6	R8	R11	R20	R22	R24	R26	RX14	RY1	RX6	RX9	RX11	RX12	UX2	UX3
P55C-133MHz	2.5V	133=66x2	V	X	V	X	V	X	X	V	V	X	V	X	X	X	X	X
P55C-150MHz	2.5V	150=60x2.5	V	X	V	V	X	X	V	V	V	X	V	X	X	X	X	X
P55C-166MHz	2.5V	166=66x2.5	V	X	V	X	X	X	V	V	V	X	V	X	X	X	X	X
TLMK-200MHz	1.8V	200=66x3	X	X	V	X	X	V	V	X	V	X	X	V	V	V	V	V
TLMK-233MHz	1.8V	233=66x3.5	X	X	V	X	V	V	X	X	V	X	X	V	V	V	V	V
TLMK-266MHz	2.0V	266=66x4	X	V	V	X	X	X	V	V	X	V	X	V	V	V	V	V

1.2.3 Audio Board

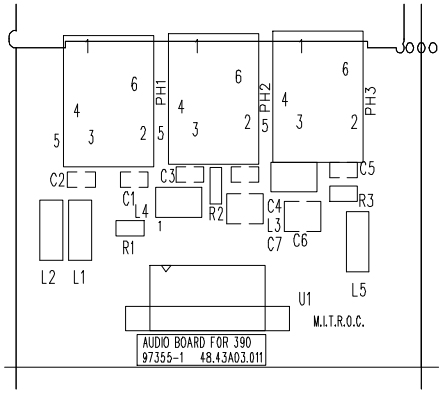


Figure 1-5 PCB No. 97355-1 Audio Board

1.2.4 Battery Board

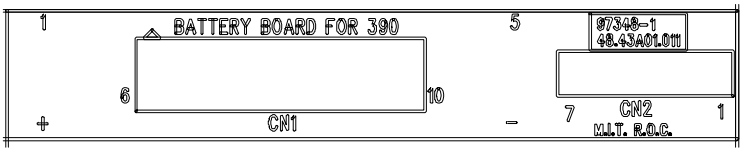


Figure 1-6 PCB No. 97348-1 Battery Board

[1] V: mount on; X: not mount on

1.2.5 Keyboard/Touchpad Board

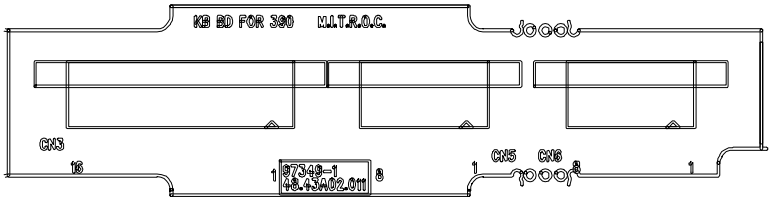


Figure 1-7 PCB No. 97349-1 Keyboard/Touchpad Board (Top View)

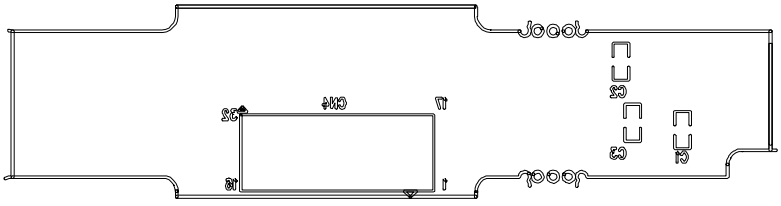
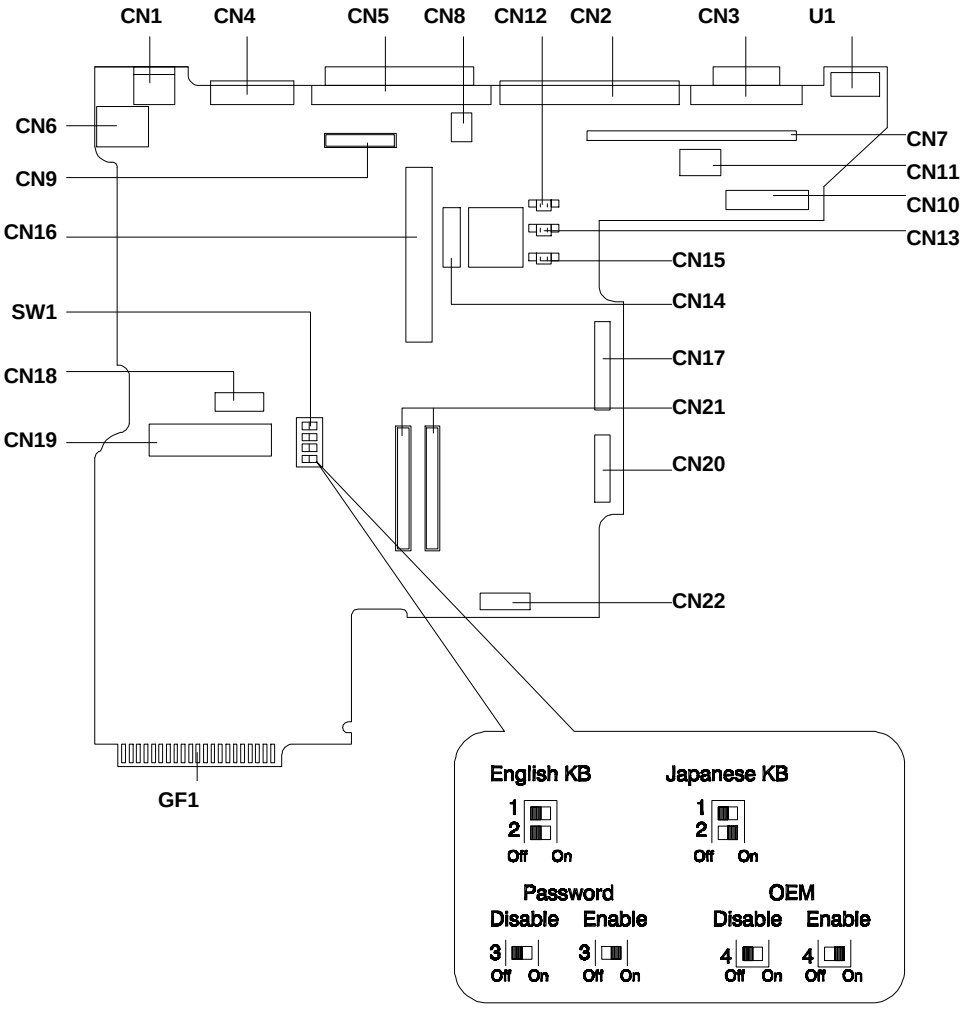


Figure 1-8 PCB No. 97349-1 Keyboard/Touchpad Board (Bottom View)

1.3 Jumpers and Connectors

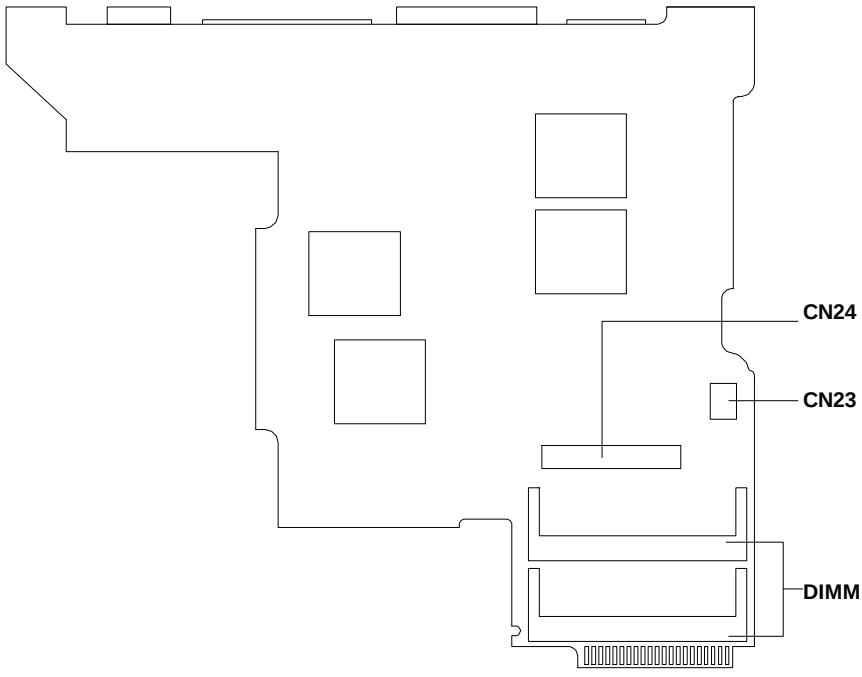
TOP VIEW



CN1	*USB port*
CN2	*Parallel port*
CN3	*Serial port*
CN4	*VGA port*
CN5	*Port replicator port*
CN6	*RJ-11 phone jack*
CN7	*DC-DC connector*
CN8	*Inverter connector*
CN9	*LCD connector*
CN10	*Charger connector*
CN11	*Charger connector*
CN12	*Fan connector*
CN13	*Internal speaker connector (left)*
CN14	*Audio board cable connector*
CN15	*Internal speaker connector (right)*
CN16	*PCMCIA socket connector*
CN17	*FDD/CD-ROM connector*
CN18	*Internal keyboard/touchpad connector*
CN19	*HDD connector*
CN20	*CD-ROM connector*
CN21	*CPU board connector*
CN22	*Battery connector*
GF1	*Golden finger for debug card*
SW1	*KB/password/logo setting switch*
U1	*FIR port*

Figure 1-9 Jumpers and Connectors (Top View)

BOTTOM VIEW



CN23 Modem connector
CN24 Modem connector
DIMM DIMM sockets

Figure 1-10 Jumpers and Connectors (Bottom View)

The following tables list the switch settings for SW1.

Table 1-2 SW1 Switch Settings

	ON		OFF
Switch 1 (Logo Screen)	OEM		Acer
Switch 2 (Password)	Bypass		Check
	Germany	**U.S.**	**Japanese**
Switch 3 (KB Language)	On	Off	Off
Switch 4 (KB Language)	Off	Off	On

1.4 Hardware Configuration and Specification

1.4.1 Memory Address Map

Table 1-3 Memory Address Map

Address Range	Definition	Function
000000 - 09FFFF	640 KB memory	Base memory
0A0000 - 0BFFFF	128 KB video RAM	Reserved for graphics display buffer
0C0000 - 0CBFFF	Video BIOS	Video BIOS
0F0000 - 0FFFFF	64 KB system BIOS	System BIOS
100000 - top limited	Extended memory	SIMM memory
FE0000 - FFFFFF	256 KB system ROM	Duplicate of code assignment at 0E0000-0FFFFF

1.4.2 Interrupt Channel Map

Table 1-4 Interrupt Channel Map

Priority	Interrupt Number	Interrupt Source
1	SMI	Power management unit
2	NMI	Parity error detected, I/O channel error
3	IRQ 0	Interval timer, counter 0 output
4	IRQ 1	Keyboard
	IRQ 2	Interrupt from controller 2 (cascade)
5	IRQ 8	Real-time clock /
6	IRQ 9	Cascaded to INT 0AH (IRQ 2) / Audio / PCMCIA
7	IRQ 10	Audio (option) / PCMCIA / Internal modem / Serial
8		communication port 2 / PCMCIA / USB
9	IRQ 11	Audio (option) / PCMCIA / Internal modem / Serial
10		communication port 1 / PCMCIA
11	IRQ 12	PS/2 mouse
12	IRQ 13	INT from coprocessor
13	IRQ 14	Hard disk controller / PCMCIA controller
14	IRQ 15	CD-ROM controller / PCMCIA controller
15	IRQ 3	Serial communication port 2 / Internal modem / Audio / PCMCIA
16	IRQ 4	Serial communication port 1 / Internal modem / Audio / PCMCIA
17	IRQ 5	Parallel port (option) / Internal modem / Audio / PCMCIA
18	IRQ 6	Diskette controller
19	IRQ 7	Parallel port (option) / Audio

1.4.3 DMA Channel Map

Table 1-5 DMA Channel Map

Controller	Channel	Address	Function
1	0	0087	Audio (option) / Audio
1	1	0083	Audio (option) / ECP / Audio / FIR
1	2	0081	Diskette
1	3	0082	Audio (option) / ECP / FIR
2	4	Cascade	Cascade
2	5	008B	Not support
2	6	0089	Not support
2	7	008A	Not support / Audio

1.4.4 I/O Address Map

Table 1-6 I/O Address Map

Address Range	Device
000 - 00F	DMA controller-1
020 - 021	Interrupt controller-1
040 - 043	Timer 1
048 - 04B	Timer 2
060 - 06E	Keyboard controller 8742 chip select
070 - 071	Real-time clock and NMI mask
080 - 08F	DMA page register
0A0 - 0A1	Interrupt controller-2
0C0 - 0DF	DMA controller-2
1F0 - 1F7	Hard disk select
220 - 22F	Audio (option) - default
230 - 23F	Audio (option)
240 - 24F	Audio (option)
250 - 25F	Audio (option)
278 - 27F	Parallel port 3
2E8 - 2EF	COM 4
2F8 - 2FF	COM 2
378, 37A	Parallel port 2
3BC - 3BE	Parallel port 1
3B4, 3B5, 3BA	Video subsystem
3C0 - 3C5	Video subsystem
3C6 - 3C9	Video DAC
3C0 - 3CF	Enhanced graphics display
3D0 - 3DF	Color graphics adapter
3E0 - 3E1	PCMCIA controller
3E8 - 3EF	COM3
3F0 - 3F7	Floppy disk controller
3F8 - 3FF	COM 1
CF8 - CFF	PCI configuration register

1.4.5 Processor

Table 1-7 Processor Specifications

Item	Specification
CPU type	P55C-133/150/166
CPU package	TCP
Switchable processor speed (Y/N)	Yes
Minimum working speed	0MHz
CPU core voltage	2.0V/2.45V/1.8V
CPU I/O voltage	2.5V/3.3V/2.5V

1.4.6 BIOS

Table 1-8 BIOS Specifications

Item	Specification
BIOS vendor	Acer
BIOS version	V3.0
BIOS in flash EPROM (Y/N)	Yes
BIOS ROM size	256KB
BIOS package type	32-pin PLCC
Same BIOS for STN color/TFT color (Y/N)	Yes

The BIOS can be overwritten/upgradeable using the "AFLASH" utility (AFLASH.EXE). Please refer to software specification section for details.

1.4.7 System Memory

Memory is upgradeable from 8 to 64 MB, employing 8-/16-/32-/64-MB[2] 64-bit soDIMMs (Small Outline Dual Inline Memory Modules). After installing the memory modules, the system automatically detects and reconfigures the total memory size during the POST routines. The following lists important memory specifications.

- Memory bus width: 64-bit
- Expansion RAM module type:144-pin, 64-bit, small outline Dual Inline Memory Module (soDIMM)
- Expansion RAM module size/configuration:
  - 8MB (1M*16x4)

[2] You can upgrade memory using 32-MB soDIMMs when these become available. Consult your dealer.

- 16MB (2M*8x8)
- 32MB (4M*16x4)
- 64MB (8M*8x8)

- Expansion RAM module speed/voltage/package: 60ns/3.3v/TSOP EDO
- EDO and fast-page mode DIMMs may be used together in a memory configuration.

The following table lists all possible memory configurations.

Table 1-9 Memory Configurations

Slot 1	Slot 2	Total Memory
8 MB	0 MB	8 MB
0 MB	8 MB	8 MB
8 MB	8 MB	16 MB
16 MB	0 MB	16 MB
0 MB	16 MB	16 MB
16 MB	8 MB	24 MB
8 MB	16 MB	24 MB
16 MB	16 MB	32 MB
32 MB	0 MB	32 MB
0 MB	32 MB	32 MB
32 MB	8 MB	40 MB
8 MB	32 MB	40 MB
32 MB	16 MB	48 MB
16 MB	32 MB	48 MB
32 MB	32 MB	64 MB
64MB	0MB	64MB
0MB	64MB	64MB
64MB	8MB	72MB
8MB	64MB	72MB
64MB	16MB	80MB
16MB	64MB	80MB
64MB	32MB	96MB
32MB	64MB	96MB
64MB	64MB	128MB

1.4.8 Second-Level Cache

This notebook has 256KB second-level (L2) cache onboard.

1.4.9 Video Memory

Table 1-10 Video RAM Configuration

Item	Specification
DRAM or VRAM	DRAM(EDO type)
Fixed or upgradeable	Fixed
Memory size/configuration	2MB (256K x 16 x 4pcs)
Memory speed	50ns
Memory voltage	3.3V
Memory package	TSOP

1.4.10 Video

Table 1-11 Video Hardware Specification

Item	Specification
Video chip	C&T65555
Working voltage	3.3V

1.4.10.1 External CRT Resolution Support

Table 1-12 Supported External CRT Resolutions

Resolution x Color on External CRT	CRT Refresh Rate		Simultaneous on TFT LCD	Simultaneous on STN LCD
	CRT only	Simultaneous	SVGA	SVGA
640x480x16	60,75,85	60	Y	Y
640x480x256	60,75,85	60	Y	Y
640x480x65,536	60,75,85	60	Y	Y
640x480x16,777,216	60,75,85	60	Y	Y
800x600x16	56,60,75,85	60	Y	Y
800x600x256	56,60,75,85	60	Y	Y
800x600x65,536	56,60,75,85	60	Y	Y
800x600x16,777,216	56,60,75,85	60	Y	Y
1024x768x16	60,75,85,86I	60	Y	Y
1024x768x256	60,75,85,86I	60	Y	Y
1024x768x65536	60,75,85,86I	60	Y	Y
1280x1024x16	60,75,86I	60	Y	Y
1280x1024x256	60,75,86I	60	Y	Y

1.4.10.2 LCD Resolution Support

Table 1-13 Supported LCD Resolutions

Resolution x Color on LCD Only	TFT LCD (SVGA)	DSTN LCD (SVGA)
640x480x16	Y	Y
640x480x256	Y	Y
640x480x65,536	Y	Y
640x480x16,777,216	Y	Y
800x600x16	Y	Y
800x600x256	Y	Y
800x600x65,536	Y	Y
800x600x16777216	Y	Y
1024x768x16	Y	Y
1024x768x256	Y	Y
1024x768x65536	Y	Y
1280x1024x16	Y	Y
1280x1024x256	Y	Y

- Maximum resolution (External CRT): 1280x1024

Using software, you can set the LCD to a higher resolution than its physical resolution, but the image shown on the LCD will pan.

1.4.11 Parallel Port

Table 1-14 Parallel Port Configurations

Item	Specification
Number of parallel ports	1
ECP support	Yes (set by BIOS setup)
Connector type	25-pin D-type
Location	Rear side
Selectable parallel port (by BIOS Setup)	• Parallel 1 (3BCh, IRQ7) • Parallel 2 (378h, IRQ7) • Parallel 3 (278h, IRQ5) • Disable

1.4.12 Serial Port

Table 1-15 Serial Port Configurations

Item	Specification
Number of serial ports	1
16550 UART support	Yes
Connector type	9-pin D-type
Location	Rear side
Selectable serial port (by BIOS Setup)	• Serial 1 (3F8h, IRQ4) • Serial 2 (2F8h, IRQ3) • Disable

1.4.13 Audio

Table 1-16 Audio Specifications

Item	Specification
Chipset	YMF715
Audio onboard or optional	Built-in
Mono or stereo	Stereo
Resolution	16-bit
Compatibility	SB-16 , Windows Sound System
Mixed sound sources	Voice, Synthesizer, Line-in, Microphone, CD
Voice channel	8-/16-bit, mono/stereo
Sampling rate	44.1 kHz
Internal microphone	No
Internal speaker / quantity	Yes / 2 pcs.
Microphone jack	Yes
Headphone jack	Yes

1.4.14 PCMCIA

PCMCIA is an acronym for Personal Computer Memory Card International Association. The PCMCIA committee set out to standardize a way to add credit-card size peripheral devices to a wide range of personal computers with as little effort as possible.

There are two type II/I or one type III PC Card slots found on the left panel of the notebook. These slots accept credit-card-sized cards that enhances the usability and expandability of the notebook.

ZV (Zoomed Video) port support allows your system to support hardware MPEG in the form of a ZV PC card.

Table 1-17 PCMCIA Specifications

Item	Specification
Chipset	TI 1250A
Supported card type	Type-II / Type-III
Number of slots	Two Type-II or one Type-III
Access location	Left side
ZV (Zoomed Video) port support	Yes

1.4.15 Touchpad

Table 1-18 Touchpad Specifications

Item	Specification
Vendor & model name	Synaptics TM3202TPD-226
Power supply voltage (V)	5 ± 10%
Location	Palm-rest center
Internal & external pointing device work simultaneously	Yes
Support external pointing device hot plug	Yes
X/Y position resolution (points/mm)	20
Interface	PS/2 (compatible with Microsoft mouse driver)

1.4.16 Keyboard

Table 1-19 Keyboard Specifications

Item	Specification
Vendor & model name	SMK KAS1901-0161R (English)
Total number of keypads	84/85 keys
Windows 95 keys	Yes, (Logo key / Application key):
Internal & external keyboard work simultaneously	Yes

1.4.16.1 Windows 95 Keys

The keyboard has two keys that perform Windows 95-specific functions. See Table 1-26.

Table 1-20 Windows 95 Key Descriptions

Key	Description
Windows logo key	Start button. Combinations with this key performs special functions, e.g.: • *Windows* + *Tab* Activate next Taskbar button • *Windows* + *E* Explore My Computer • *Windows* + *F* Find Document • *Windows* + *M* Minimize All • *Shift* + *Windows* + *M* Undo Minimize All • *Windows* + *R* Display Run dialog box
Application key	Opens the application's context menu (same as right-click).

1.4.17 FDD

Table 1-21 FDD Specifications

Item	Specification		
Vendor & model name	Mitsumi D353F2		
Floppy Disk Specifications			
Media recognition	2DD (720K)	2HD (1.2M, 3-mode)	2HD (1.44M)
Sectors / track	9	15	18
Tracks	80	80	80
Data transfer rate (Kbits/s)	250 300	500	500
Rotational speed (RPM)	300 360	360	300
Read/write heads	2		
Encoding method	MFM		
Power Requirement			
Input Voltage (V)	+5 ± 10%		

1.4.18 HDD

Table 1-22 HDD Specifications

Item	Specification		
Vendor & Model Name	Hitachi DK225A-21	IBM DTNA22160	IBM DDLA21620
Drive Format			
Capacity (MB)	2160	2160	1620
Bytes per sector	512	512	512
Logical heads	16	16	16
Logical sectors	63	63	63
Logical cylinders	4889	4200	3152
Physical read/write heads	6	6	3
Disks	3	3	2
Spindle speed (RPM)	4464	4000	4000
Performance Specifications			
Buffer size (KB)	128	96	96
Interface	ATA-3(IDE)	ATA-2	ATA-2
Data transfer rate (disk-buffer, Mbytes/s)	5.7 ~ 9.0	5 ~ 7.7	5 ~ 8.3
Data transfer rate (host-buffer, Mbytes/s)	16.6 /33.3 (max., PIO mode 4)	16.6 (max., PIO mode 4)	16.6 (max., PIO mode 4)
DC Power Requirements			
Voltage tolerance (V)	5 ± 5%	5 + 5%	5 ± 5%

1.4.19 CD-ROM

Table 1-23 CD-ROM Specifications

Item	Specification
Vendor & Model Name	Panasonic KMEUJDA110
Performance Specification	
Speed (KB/sec)	2100 (14X ave. speed)
Access time (ms)	150 (Typ.)
Buffer memory (KB)	128
Interface	Enhanced IDE (ATAPI) compatible
Applicable disc format	CD-DA, CD-ROM, CD-ROM XA (except ADPCM), CD-I, Photo CD (Multisession), Video CD, CD+
Loading mechanism	Soft eject (with emergency eject hole)
Power Requirement	
Input Voltage (V)	5

1.4.20 Battery

Table 1-24 Battery Specifications

Item	Specification	
Battery gauge on screen	Yes, by hotkey	Yes, by hotkey
Vendor & model name	Toshiba BTP-031	Sony BTP-T31
Battery type	NiMH	Li-Ion
Cell capacity (mAH)	3500	1400
Cell voltage (V)	1.2	3.6
Number of battery cell	9-cell	9-Cell
Package configuration	9 serial	3 serial, 3 parallel
Package voltage (V)	10.8	10.8
Package capacity (WAH)	3500	4200
Second battery	No	No

1.4.21 Charger

To charge the battery, place the battery pack inside the battery compartment and plug the AC adapter into the notebook and an electrical outlet. The adapter has three charging modes:

- Rapid mode

  The notebook uses rapid charging when power is turned off and a powered AC adapter is connected to it. In rapid mode, a fully depleted battery gets fully charged in approximately two hours.

- Charge-in-use mode

  When the notebook is in use with the AC adapter plugged in, the notebook also charges the battery pack if installed. This mode will take longer to fully charge a battery than rapid mode. In charge-in-use mode, a fully depleted battery gets fully charged in approximately six to eight hours.

- Trickle mode

  The adapter charges the battery pack for two hours using trickle current 380mA, then shifts to 1/10 duty pulse trickle charge to keep the battery capacity at 100%.

Table 1-25 Charger Specifications

Item	Specification
Vendor & model name	Ambit T62.069.C.00
Input voltage (from adapter, V)	0-24V
Output current (to DC/DC converter, A)	3 (max.)
Battery Low Voltage	
Battery Low 1 level (V)	10.16 (typ., for NiMH) 8.566 (typ., for LIB)
Battery Low 2 level (V)	10.279 (typ., for NiMH) 8.185 (typ., for LIB)
Battery Low 3 level (V)	9.137 (typ., for NiMH) 7.709 (typ., for LIB)
Charge Current	
Background charge (charge even system is still operative, A)	0.8 (typ.)
Normal charge (charge while system is not operative, A)	2.0 (typ.)
Charging Protection	
Maximum temperature protection (ºC)	60
Maximum voltage protection (V)	16.7V±0.2V
Over voltage protection	13V±0.15

1.4.22 DC-DC Converter

DC-DC converter generates multiple DC voltage level for whole system unit use.

Table 1-26 DC-DC Converter Specifications

Item	Specification					
Vendor & model name	Ambit T62.041.C.00					
Input voltage (Vdc)	8~21					
Output Rating	**5V**	**3.3V**	**2.9V (2.9 /3.1 /3.3V)**	**+12V**	**+6V**	**5VSB**
Current (w/ load, A)	0~3.2	0~3.3	0~4.2	0~0.15	0~0.1	0.005
Voltage ripple (max., mV)	50	50	50	100	300	75
Voltage noise (max., mV)	100	100	100	200	500	250
OVP (Over Voltage Protection, V)	6.1~8.0	4.2~6.2	3.3-5.2 V	-	-	-

1.4.23 DC-AC Inverter

DC-AC inverter is used to generate very high AC voltage, then supply to LCD CCFT backlight use, and is also responsible for the control of LCD brightness. Avoid touching the DC-AC inverter area while the system unit is turned on.

Table 1-27 DC-AC Inverter Specifications

Item	Specification		
Vendor & model name	Ambit T62.071.C.00		
Input voltage (V)	6.8(in.)	-	22(max.)
Input current (mA)	-	-	750 (max.)
Output voltage (Vrms, no load)	1000 (min.)	-	1600 (max.)
Output voltage frequency (kHz)	40 (min.)	-	65 (max.)
Output current (mArms)	1.0~5.5 (min.)	1.5~6.1 (typ.)	2.0~6.7 (max.)

1.4.24 LCD

Table 1-28 LCD Specifications

Item	Specification		
Vendor & model name	HITACHI LMG9980ZWCC-01	TORiSAN LM-JK53-22NFR-A	HITACHI TX31D21VC
Mechanical Specifications			
LCD display area (diagonal, inch)	12.1	12.1	12.1
Display technology	STN	STN	TFT
Resolution	SVGA (800x600)	VGA (800x600)	SVGA (800x600)
Supported colors	--	--	262,144 colors
Optical Specification			
Contrast ratio	35 (typ.)	40 (typ.)	80 (typ.)
Brightness (cd/m^2)	70 (typ.)	70 (typ.)	70 (typ.)
Brightness control	keyboard hotkey	keyboard hotkey	keyboard hotkey
Contrast control	using keyboard hotkey	using keyboard hotkey	none
Electrical Specification			
Supply voltage for LCD display (V)	3.3 or 5 (typ.)	3.3 or 5 (typ.)	3.0 ~ 3.6 (typ.)
Supply voltage for LCD backlight (Vrms)	650 (typ.)	630 (typ.)	595(typ.), 660(max)

1.4.25 AC Adapter

Table 1-29 AC Adapter Specifications

Item	Specification
Vendor & model name	Delta ADP-45GB Rev. E3, E5
Input Requirements	
Nominal voltages (Vrms)	90 - 264
Nominal frequency (Hz)	47 - 63
Frequency variation range (Hz)	47 - 63
Maximum input current (A, @90Vac, full load)	1.5 A
Inrush current	The maximum inrush current will be less than 50A and 100A when the adapter is connected to 115Vac(60Hz) and 230Vac(50Hz) respectively.
Efficiency	It should provide an efficiency of 83% minimum, when measured at maximum load under 115V(60Hz).
Output Ratings (CV mode)	
DC output voltage (V)	+19.0V~20.5V
Noise + Ripple (mV)	300mvp-pmax (20Mhz bandwidth)
Load (A)	0 (min.) 2.4 (max.)
Output Ratings (CC mode)	
DC output voltage (V)	+12 ~+19
Constant output (A)	2.75 ± 0.2
Dynamic Output Characteristics	
Turn-on delay time (s, @115Vac)	2
Hold up time (ms; @115 Vac input, full load)	5 (min.)
Over Voltage Protection (OVP, V)	26
Short circuit protection	Output can be shorted without damage
Electrostatic discharge (ESD, kV)	±15 (at air discharge)
Dielectric Withstand Voltage	
Primary to secondary	3000 Vac (or 4242 Vdc), 10 mA for 1 second
Leakage current	0.25 mA maximum @ 254 Vac, 60Hz.
Regulatory Requirements	
Internal filter meets: 1. FCC class B requirements. (USA) 2. VDE 243/1991 class B requirements. (German) 3. CISPR 22 Class B requirements. (Scandinavia) 4. VCCI class II requirements. (Japan)	

1.5 Software Configuration and Specification

1.5.1 BIOS

The BIOS is compliant to PCI v2.1, APM v1.2, E-IDE and PnP specification. It also defines the hotkey functions and controls the system power-saving flow.

1.5.1.1 Keyboard Hotkey Definition

The notebook supports the following hotkeys.

Table 1-30 Hotkey Descriptions

Hotkey	Icon	Function	Description
Fn-Esc		Hotkey Escape	Exits the hotkey control.
Fn-F1	?	Hotkey Help	Displays the hotkey list and help. Press | to exit the screen.
Fn-F2		Brightness Control  Contrast Control 	Toggles between brightness control and contrast control. Press the scale hotkeys (Fn- →and Fn -←) to increase and decrease the brightness or contrast level. Notebooks with TFT displays do not show the brightness control icon.
Fn-F3		Display Toggle	Switches display from LCD to CRT to both LCD and CRT.
Fn-F4		Battery Gauge 	Displays the battery gauge.
Fn-F5		Volume Control 	Press the scale hotkeys (Fn-→ and Fn-←) to increase and decrease the output level.
Fn-F6		Setup	Gains access to BIOS Setup's Advanced System Configuration parameters.
Fn-F7	Z^Z	Hibernation/Standby	Enters hibernation mode if the 0-volt suspend function is installed and enabled; otherwise, the notebook enters standby mode.
Fn-→		Scale Increase	Increases the setting of the current icon.
Fn-←		Scale Decrease	Decreases the setting of the current icon.
Fn-T		Toggle Touchpad	Turns the internal touchpad on and off.

When the available hotkey is toggled, the system will issue a beep to enter the assigned process.

1.5.1.2 MultiBoot

The system can boot from the FDD, External FDD, HDD, CD-ROM. The user can select the desired booting process to boot the system. If the CD-ROM is bootable, the BIOS will override the other process to boot the system directly.

1.5.1.3 Power Management

This computer has a built-in power management unit that monitors system activity. System activity refers to any activity involving one or more of the following devices: keyboard, mouse, floppy drive, hard disk, peripherals connected to the serial and parallel ports, and video memory. If no activity is detected for a period of time (called an inactivity time-out), the computer stops some or all of these devices in order to conserve energy.

This computer employs an innovative power management technique called Heuristic Power Management or HPM. HPM allows the computer to provide maximum power conservation and maximum performance at the same time.

Power management methods used by most computers are timer-based. You set inactivity time-out values for the display, hard disk, and other devices. The computer then "sleeps" when these time-outs elapse. The problem with this is that no two users are alike. Each of us has his or her own habits when using the computer, which makes timer-based power management ineffective.

With HPM, your computer manages its power according to the way you use your computer. This means the computer delivers maximum power when you need it, and saves power when you don't need the maximum — all without your intervention. There are no timers to set, because the HPM system figures out everything for you.

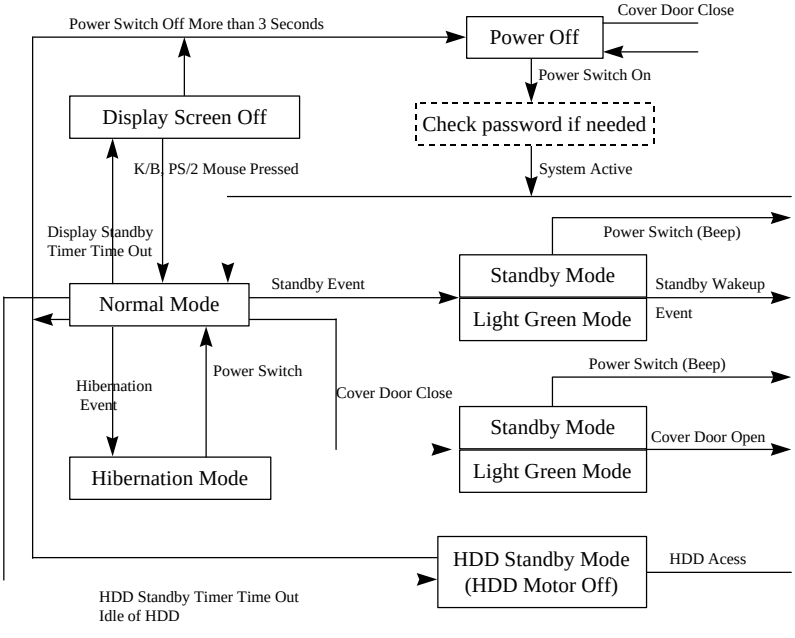


Figure 1-11 Power Management Block Diagram

ON MODE

Normal full-on operation

STANDBY MODE

The computer consumes very low power in standby mode. Data remain intact in the system memory until battery is drained.

Warning: Unstored data is lost when you turn off the computer power in standby mode or when the battery is drained.

Table 1-31 Standby Mode Conditions and Descriptions

Condition	Description
The condition to enter Standby Mode	There are two necessary conditions for the computer to enter standby mode: • Heuristic Power Management Mode must be set to [ENABLED]. • System Sleep State must be set to [STANDBY]. In this situation, the following are ways to enter standby mode: • Pressing the sleep hot key Fn-F7 • If the waiting time determined by the computer's HPM unit elapses without any system activity. • Closing the display cover. • With the System Sleep State is set to [HIBERNATION], the computer also enters standby mode if the hibernation file (Sleep Manager) is invalid or not present. • "Hard Disk Drive" is [Disabled] in System Security of BIOS SETUP. • "Hard Disk 0" is [None] in Basic System Configuration of BIOS SETUP. **Note:** If the computer detects a PC I/O card installed in the PC card slots, the computer "sleeps" (light green mode) to maintain your communications connection. It will not enter standby mode.
The condition of Standby Mode	• Issue a beep. • Light standby LED with 1 Hz frequency. • Disable the mouse, serial and the parallel port. • The keyboard controller, HDD and VGA enter the standby mode. • Stop the CPU internal clock. • All the functions are disabled except the keyboard, battery low warning and modem ring wake up from standby (if enabled).
The condition back to On Mode	Any one of following activities will let system back to Normal Mode: • Any keystroke (Internal KB or External KB) • Any active pointing device (internal or external, PS/2 or serial or USB) • Resume Timer matched • Opening the display cover if you closed the display cover to enter Standby mode. • Modem ring

LIGHT GREEN MODE

The notebook consumes very low power in light green mode. Data and I/O connections remain intact in the system memory until battery is drained.

Table 1-32 Light Green Mode Conditions and Descriptions

Condition	Description
The condition to enter Light Green Mode	• PCMCIA I/O Card detected and occupy resources (Non Cardbus mode). • HPM timer times out or cover close or APM standby / suspend function calls.
The condition of Light Green Mode	• Issue a beep. • Only HDD, VGA enter standby
The condition back to On Mode	Any one of following activities will let system back to Normal Mode: • Any keystroke (Internal KB or External KB) • Modem ring.

HIBERNATION MODE

In hibernation mode, all power shuts off (the computer does not consume any power). The computer saves all system information onto the hard disk before it enters hibernation mode. Once you turn on the power, the computer restores this information and resumes where you left off upon leaving hibernation mode.

If the computer beeps but does not enter hibernation mode after pressing the sleep hot key, it means the operating system will not allow the computer to enter the power saving mode.

Do not change any devices (such as add memory or swap hard disks when the computer is in hibernation mode.

If the computer detects a PC I/O card installed in the PC card slots, the computer enters light green mode to maintain your communications connection. It will not enter standby nor hibernation mode.

Table 1-33 Hibernation Mode Conditions and Descriptions

Condition	Description
The condition to enter Hibernation Mode	There are two necessary conditions for the computer to enter standby mode: • Heuristic Power Management Mode must be set to [ENABLED]. • System Sleep State must be set to [HIBERNATION]. • The hibernation file created by Sleep Manager must be present and valid. In this situation, the following are ways to enter hibernation mode: • Pressing the sleep hot key Fn-F7 • "Hard Disk Drive" is not [Disabled] in System Security of BIOS SETUP. • "Hard Disk 0" is not [None] in Basic System Configuration of BIOS SETUP. • If the waiting time determined by the computer's HPM unit elapses without any system activity. • If a battery low condition takes place, the computer enters hibernation mode in about three minutes. The Sleep Upon Battery-low parameter in Setup must be set to [ENABLED]. • Invoked by the operating system power saving modes
The condition of Hibernation Mode	• Except the RTC, KB controller and power switch, all the system components are off.
The condition back to On Mode	• Pressing the power switch. • Resume Timer matched

DISPLAY STANDBY MODE

Screen activity is determined by the keyboard, the built-in touchpad, and an external PS/2 pointing device. If these devices are idle for the period determined by the computer's HPM unit, the display shuts off until you press a key or move the touchpad or external mouse.

Table 1-34 Display Standby Mode Conditions and Descriptions

Condition	Description
The condition to enter Display Standby Mode	• Pointing device is idle until Display Standby Timer times-out or LCD cover is closed.
The condition of Display Standby Mode	• All the system components are on except LCD backlight and CRT horizontal frequency output (if CRT is connected)
The condition back to On Mode	• Any keystroke (Internal KB or External KB) • Pointing device activity

The VGA BIOS should support DPMS (Desktop Power Management System) for the standby and hibernation mode function call. When the Display Standby Timer expires, the system BIOS will execute the DPMS service routines.

HARD DISK STANDBY MODE

The hard disk enters standby mode when there are no disk read/write operations within the period of time determined by the computer's HPM unit. In this state, the power supplied to the hard disk is reduced to a minimum. The hard disk returns to normal once the computer accesses it.

Table 1-35 Hard Disk Standby Mode Conditions and Descriptions

Condition	Description
The condition to enter HDD Standby Mode	Display Standby HPM timer times-out or LCD cover is closed.
The condition of HDD Standby Mode	All the system components are on except HDD spindle motor
The condition back to On Mode	Any access to HDD

BATTERY LOW

When the battery capacity is low and no adapter is plugged in, the system will generate the following battery low warning:

- Flash power LED with 1 Hz.
- Issue 4 short beeps per minute (if enabled in setup).
- If the AC adapter does not plug in within 3 minutes and the "Standby/Hibernation upon Battery-low" in BIOS SETUP is enabled, the system will enter Standby/0-Volt Hibernation Mode. The battery low warning will stop as soon as the AC adapter is plugged into the system.

THE AUTODIM PROCESS OF THE LCD BRIGHTNESS

The notebook has a unique **"automatic dim"** power saving feature. When the notebook is using AC power and you disconnect the AC adapter from the notebook, the system "decides" whether or not to automatically dim the LCD backlight to save power.

If the LCD backlight is too bright, the system automatically adjusts it to a manageable level; otherwise, the level stays the same. If you want a brighter picture, you can then adjust the brightness and contrast level using hotkeys (Fn-F2).

If you reconnect AC power to the system, the system automatically adjusts the LCD backlight to its original level — the brightness and contrast level before disconnecting the AC adapter. If you adjusted the brightness and contrast level after disconnecting AC power, the level stays the same after you reconnect the AC adapter.

There are two reasons for the notebook to have the LCD AutoDim feature. The first is to save the power during the notebook is operating under the DC mode. The second is to save the "favorite" brightness parameter set by the user.

The following processes are the basic methods used to implement the LCD brightness AutoDim.

1. If the original brightness is over 75% and the AC power is on-line, the BIOS will change the brightness to 75% after the AC power is off-line.

2. If the original brightness is below 75%, the brightness maintains the same level even if the AC power is off-line.

3. If the brightness is already changed by the hotkey under DC power, it will not be changed after the AC power is plugged in.

4. If the brightness is not changed by the hotkey under DC power, the brightness will be changed back to the old setting — the previous brightness parameter under AC power.

5. If the previous brightness parameter does not exist, the brightness will not be changed in process 4.

1.5.2 Drivers, Applications and Utilities

The notebook comes preloaded with the following software:

- Windows 95[3]
- System utilities and application software[4]
  - Sleep Manager utility
  - Display drivers
  - Audio drivers
  - PC Card slot drivers and applications
  - Other third-party application software

Table 1-36 Location of Drivers in the System Utility CD

Device Category	Function	Location
Sound, video and game controllers	Audio	ENGLISH\WIN95\AUDIO\
Mouse	Mouse	ENGLISH\WIN95\MOUSE\
Display adapters	Video	ENGLISH\WIN95\VGA\
PCMCIA	Zoomed Video Port	English\Win95\PCMCIA\

[3] In some areas, a different operating system may be pre-loaded instead of Windows 95.

[4] The system utilities and application software list may vary.

To re-install applications under Windows 95, click on Start, then Run…. Based on the location of the application, run the setup program to install the application. The following table lists the applications and their locations:

Table 1-37 Location of Applications in the System Utility CD

Name	Function	Location
Sleep Manager	0V Suspend utility	ENGLISH\WIN95\SLEEPMGR\
Y-Station	Audio application	ENGLISH\WIN95\Ystation
SafeOFF	Protect if user accidentally press the power switch	ENGLISH\WIN95\SAFEOFF

Drivers for Windows 3.x and Windows NT are also found in the System Utility CD if you should need them.

1.6 Block Diagrams

1.6.1 System

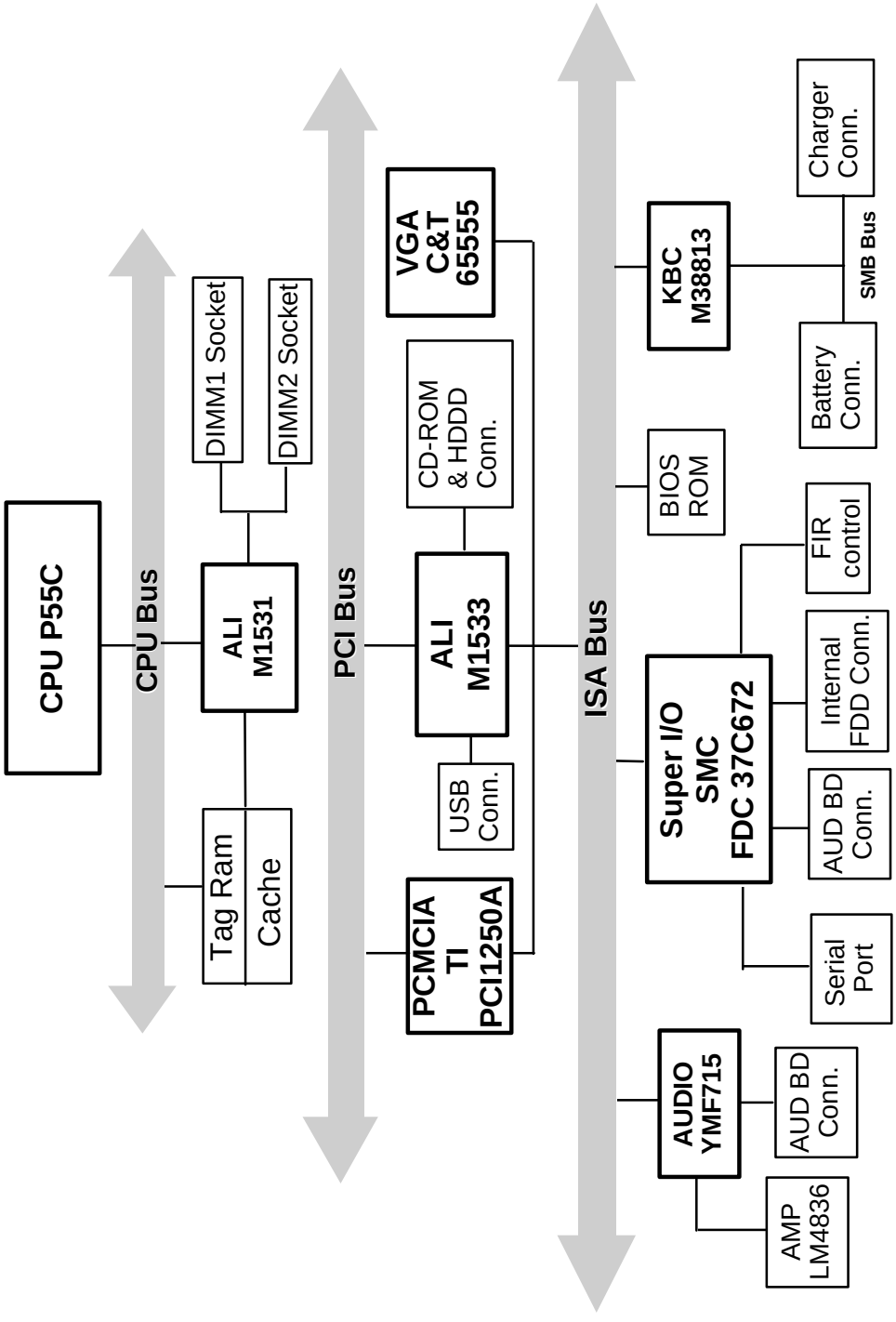


Figure 1-12 System Block Diagram

1.6.2 Clock

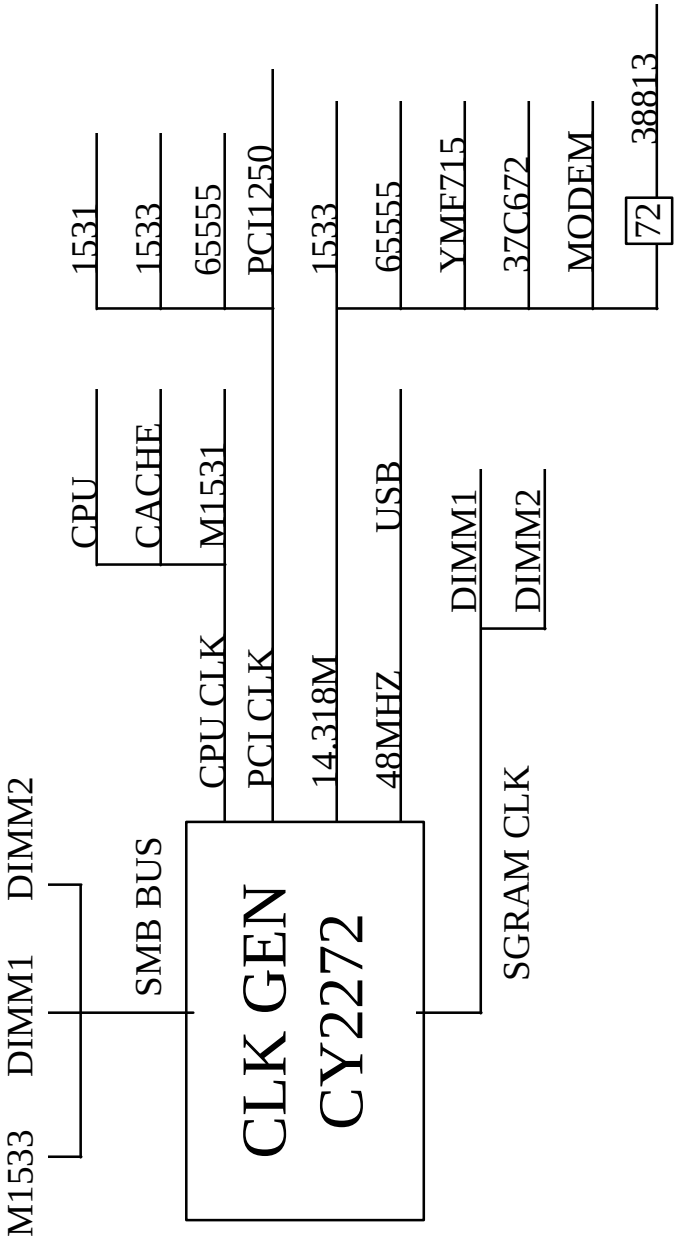


Figure 1-13 Clock Block Diagram

1.7 Environmental Requirements

Table 1- 38 Environmental Requirements

Item	Specification
Temperature	
Operating (ºC)	+5~ +35
Non-operating(ºC)	-20 ~ +60
Humidity	
Operating (non-condensing)	20% ~ 80%
Non-operating (non-condensing)	20% ~ 80%
Operating Vibration (unpacked)	
Operating	5 - 25.6Hz, 0.38mm; 25.6 - 250Hz, 0.5G
Sweep rate	0.5 octave / minute
Number of test cycles	2 / axis (X,Y,Z)
Non-operating Vibration (unpacked)	
Non-operating	5 - 27.1Hz, 0.6G; 27.1 - 50Hz, 0.41mm; 50-500Hz, 2G
Sweep rate	0.5 octave / minute
Number of text cycles	4 / axis (X,Y,Z)
Non-operating Vibration (packed)	
Non-operating	5 - 62.6Hz, 0.51mm; 62.6-500Hz, 4G
Sweep rate	0.5 octave / minute
Number of text cycles	4 / axis (X,Y,Z)
Shock	
Operating	5G peak, 11±1ms, half-sine
Non-operating (unpacked)	40G peak, 11±1ms, half-sine
Non-operating (packed)	50G peak, 11±1ms, half-sine
Altitude	
Operating	10,000 feet (5°C ~ 40°C)
Non-operating	40,000 feet (-10°C ~ 60°C)
ESD	
Air discharge	8kV (no error) 12.5kV (no restart error) 15kV (no damage)
Contact discharge	4kV (no error) 6kV (no restart error) 8kV (no damage)

1.8 Mechanical Specifications

Table 1-39 Mechanical Specifications

Item	Specification
Weight FDD model CD-ROM model	(includes battery) 2.77 kg. (6.11 lb.) 2.8 kg. (6.2 lb.)
Dimensions (main footprint)	W x D x H 311.5mm x 236/246mm x 46.5mm (12.26” x 9.29”/9.69” x 1.83”)

Major Chips Description

This chapter discusses the major chips used in the notebook.

Table 2-1 Major Chips List

Component	Vendor	Description
PCI 1250A	TI	PC Card controller chip
Aladdin IV (M1531/M1533)	ALi	System Architecture chipset
FDC37C672	SMC	Super I/O controller chip
65555	C&T	Video controller chip
M38813		Keyboard controller chip
YMF715B-S	Yamaha	Audio chip

2.1 PCI 1250A

The Texas Instruments PCI1250A is a high-performance PC Card controller with a 32-bit PCI interface. The device supports two independent PC Card sockets compliant with the 1995 PC Card Standard. The PCI1250A provides a rich featured set which make it the best choice for bridging between PCI and PC Cards in both notebook and desktop computers. The 1995 PC Card Standard retains the 16-bit PC Card specification defined in PCMCIA Release 2.1, and defines the new 32-bit PC Card, CardBus, capable of full 32-bit data transfers at 33 MHz. The PCI1250A supports any combination of 16-bit and CardBus PC Cards in the two sockets, powered at 5V or 3.3V as required.

The PCI1250A is compliant with the PCI Local Bus Specification Revision 2.1, and its PCI interface can act as either a PCI master device or a PCI slave device. The PCI bus mastering is initiated during 16-bit PC Card DMA transfers, or CardBus PC Card bridging transactions.

All card signals are internally buffered to allow hot insertion and removal without external buffering. The PCI1250A is register compatible with the Intel 82365SL-DF ExCA controller. The PCI1250A internal data-path logic allows the host to access 8-, 16-, and 32-bit cards using full 32-bit PCI cycles for maximum performance. Independent buffering and a pipeline architecture provide an unsurpassed performance level with sustained bursting. The PCI 1250A can also be programmed to accept fast posted writes to improve system-bus utilization.

The PCI1250A provides an internally buffered zoom video path. This reduces the design effort of PC board manufacturers to add a ZV compatible solution and guarantees compliance with the CardBus loading specifications. Multiple system interrupt signaling options are provided including: parallel PCI, parallel ISA, serialized ISA, and serialized PCI. Furthermore, general purpose inputs and outputs are provided for the board designer to implement sideband functions. Many other features are designed into the PCI1250A such as socket activity LED outputs, and are discussed in detail throughout the design specification.

An advanced CMOS process is used to achieve low system power consumption while operating at PCI clock rates up to 33MHz. Several low-power modes allow the host power management system to further reduce power consumption.

2.1.1 Features

- PCI Power Management Compliant
- ACPI 1.0 Compliant
- Packaged in a 256-pin BGA
- PCI Local Bus Specification Rev. 2.1 Compliant
- 1995 PC Card Standard Compliant
- 3.3 Volt Core Logic with Universal PCI Interfaces Compatible with 3.3 Volt and 5 Volt PCI Signaling Environments
- Mix and Match 5V/3.3V PC Card16 Cards and 3.3V CardBus Cards
- Supports Two PC Card™ or CardBus Slots with Hot Insertion and Removal
- Uses Serial Interface to TI TPS2206A Dual Power Switch

- Supports Burst Transfers to Maximize Data Throughput on both PCI Buses
- Supports Serialized IRQ with PCI Interrupts
- 8-Way Legacy IRQ Multiplexing
- System Interrupts can be Programmed as PCI-style or ISA IRQ-style
- ISA IRQ interrupts can be Serialized onto a single IRQSER pin
- EEPROM Interface for Loading Subsystem ID and Subsystem Vendor ID
- Pipelined Architecture allows Greater than 130 Mbytes per second throughput from CardBus to PCI and from PCI to CardBus
- Supports Zoom Video with Internal Buffering
- Programmable Output Select for CLKRUN
- Four General Purpose I/O's
- Multi-function PCI Device with Separate Configuration Space for each Socket
- Five PCI Memory Windows and Two l/O Windows Available to each PC Card16 Socket
- Two I/O Windows and Two Memory Windows Available to each CardBus Socket
- ExCA™-Compatible Registers are Mapped in Memory and I/O Space
- Supports Distributed DMA and PC/PCI DMA
- Intel™- 82365SL-DF Register Compatible
- Support 16-bit DMA on both PC Card Sockets
- Supports Ring indicate, SUSPEND, and PCI CLKRUN
- Advanced Submicron, Low-Power CMOS Technology
- Provides VGA / Palette Memory and I/O, and Subtractive Decoding Options
- LED Activity Pins
- Supports PCI Bus Lock

2.1.2 Block Diagram

A simplified block diagram of the PCI1250 is provided in following figure. The PCI interface includes all address/data and control signals for PCI protocol. The interrupt interface includes terminals for parallel PCI, parallel ISA, and serialized PCI & ISA signaling. The ring indicate terminal is included in the interrupt interface, since it's function is to perform system wake-up on incoming PC Card modem rings. Miscellaneous system interface terminals include GPIO signals, PC/PCI DMA support signals, and socket activity LED signals.

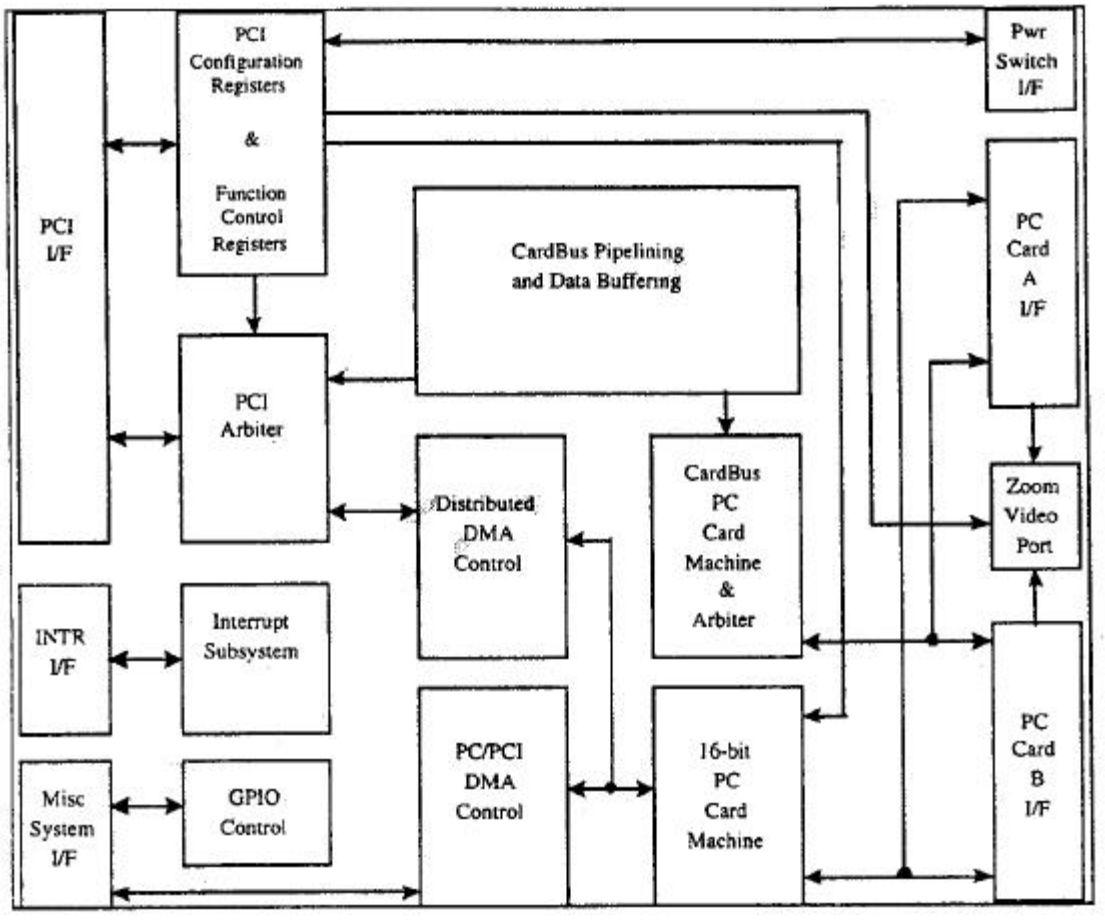


Figure 2-1 PCI1250 Block Diagram

2.1.3 Terminal Functions

This section describes the PCI1250A terminal functions. The terminals are grouped in tables by functionality such as PCI system function, power supply function, etc. for quick reference. The terminal numbers are also listed for convenient reference.

Table 2-2 PCI1250 Terminal Functions

Name	No.	I/O Type	Function
Power Supply Terminals			
GND	A01, D04, D08, D13, 17, H04, H17, N04, N17, U04, U08, U13, U17,	I	Device ground terminals
VCC	D06, D11, D15, F04, F17, 04, L17, R04, R17, U06, U10, U15	I	3.3 V Power supply terminal for core logic.
VCCA	K02, R03, W05	I	Rail Power Input for PC Card A Interface. Indicates Card A signaling environment.
VCCB	B16, C10, F18	I	Rail Power Input for PC Card B Interface. Indicates Card A signaling environment.
VCCI	V10	I	Rail power Input for interrupt subsystem interface and miscellaneous l/O. Indicates signaling level of the following inputs and shared outputs: IRQSER, PCGNT. PCREQ SUSPENCX, SPKROUT, GPI01:0, IRQMUX7:0, INTA, INTB CLOCK. DATA, LATCH, and RI_OUT
VCCP	K20, P18, V15, W20	I	Rail power input for PCI signaling.
VCCZ	A04, D01	I	Rail power input for the Zoom Video Interface
PCI System Terminals			
PCLK	J17	I	PCI bus clock. Provides timing fot all transactions on the PCI bus. All PCI signals are sampled at the rising edge H PCLK.
PRST	J19	I	PCI reset When the PCI bus reset is asserted the PRST signal causes the PCI 1 250A to 3-state all output buffers and reset all internal registers. When PRST is asserted, the device is completely nonfunctional. After PRST is deasserted, the PCI1250A is in its default state. When the SUSPEND mode is enabled, the device is protected from the PRST clearing the internal registers. An outputs are 3-statea but the contents of the registers are preserved
CLKRUN	J18	O	PCI clock run. This signal is used by the central resource to request permission to stop the PCI clock or to slow it down, and the PCI1250A responds accordingly.

Table 2-2 PCI1250 Terminal Functions

Name	No.	I/O Type	Function
PCI Address and Data Terminals			
AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 AD23 AD22 AD21 AD20 AD19 AD18 AD17 AD16 AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0	K18 K19 L20 L18 L19 M20 M19 M18 N19 N18 P20 P19 R20 R19 P17 R18 V18 Y19 W18 V17 U16 Y18 W17 V16 W16 U14 Y16 W15 V14 Y15 W14 Y14		PCI address data bus. These signals make up the multiplexed PCI address and data bus on the primary interface. During the address phase of a primary bus PCI cycle, AD31:0 contain a 32-bit address or other destination. During the data phase AD31 0 contain data.
C/BE3 C/BE2 C/BE1 C/BE0	M17 T20 W19 Y17	I/O	PCI bus commands and byte enables. These signals are multiplexed on the same PCI terminals. During address phase of a primary bus PCI cycle, C/BE3:0 define the bus command. During the data phase, this four-bit bus is used as byte enables. The byte enables determine which byte paths of the full 32-bit data bus carry meaningful data. C/BE0 applies to byte 0 (AD7:0), C/BE1 applies to byte 1 (AD15:8), C/be2 applies to byte 2 (AD23:16) and C/BE3 applies to byte 3 (AD31:24).
PAR	Y20	I/O	PCI bus party In all PCI bus read and write cycles the PCI1250A calculates even parity across the AD31:0 and C/BE3:0 buses. As an initiator during PCI cycles, the PCI1250A outputs this parity indicator with a one PCLK delay. As a target during PCI cycles. the calculated parity is compared to the initiators parity indicator. A miscompare can result in the assertion of a parity error (PERR).

Table 2-2 PCI1250 Terminal Functions

Name	No.	I/O Type	Function
PCI Interface Control Terminals			
DEVSE	V20	I/O	PCI device select. The PCI1250A asserts this signal to claim a PCI cycle as the target device. As a PCI initiator on the bus. the PCI1250A monitors this signal until a target responds. If no target responds before time-out occurs, then the PCI1250A will terminate the cycle with an initiator abort.
FRAME	T19	I/O	PCI cycle frame. This signal is driven by the initiator of a bus cycle. FRAME is asserted to indicate that a bus transaction is beginning, and data transfers continue while this signal is asserted. When FRAME is deasseerted the PCI bus transaction is in the final data phase.
GNT	J20	I	PCI bus grant. This signal is driven by the PCI bus arbiter to grant the PCI1250A access to the PCI bus after current data transaction has completed. This signal may or may not follow a PCI bus request depending upon the PCI bus parking algorithm.
GPIO2/LOCK	V19	I/O	PCI bus general purpose I/O pins or PCI bus lock. These pins are can be configured as PCI LOCK and used to gain exclusive access downstream. Since this functionality is not typically used, a general purpose I/O may be accessed through this terminal. This terminal defaults to a general purpose input, and maybe configured through the *GPIO2 Control Register*
IDSEL	N20	I	Initalization device select. IDSEL selects the PCI1250A during configuration space accesses. IDSEL can be connected to one of the upper 24 PCI address lines on the PCI bus.
IRDY	T18	I/O	PCI initiator ready. IRDY indicates the PCI bus initiator's ability to complete the current data phase of the transaction. A data phase is completed upon a rising edge of PCLK where both IRDY and TRDY are asserted. Until IRDY and TRDY are both sampled asserted. wait states are inserted.
PERR	U18	I/O	PCI parity error indicator. This signal is driven by a PCI device to indicate that calculated parity does not match PAR, when PERR is enabled through bit 6 of the command register.
REQ	K17	O	PCI bus request. Asserted by the PCI1250A to request access to the PCI bus as an initiator.
SERR	U19	O	PCI system error. Output that is pulsed from the PCI1250A, when enabled through the command register, indicating a system error has occurred. The PCI 1250A needs not be the target of the PCI cycle in order to assert this signal. When SERR is enabled in the control register, this signal will also pulse indicating that address parity error has occurred on a CardBus interface.

Table 2-2 PCI1250 Terminal Functions

Name	No.		I/O Type	Function
STOP	T17		I/O	PCI cycle stop signal. This signal is driven by a PCI target to request the initiator to stop the current PCI bus tranaction. This signal is used for target disconnects and is commonly asserted by target devices which do not support burst data transfers.
TRDY	U20		I/O	PCI target ready. TRDY indicates the primary bus target s ability to complete the current data phase of the transaction. A data phase is completed upon a rising edge of PCLK where both IRDY and TRDY are asserted. Until both IRDY and TRDY are asserted, wait states are inserted.
PC Card 16 Address And Data Terminals (Slot A And Slot B)				
	Slot A[1]	**Slot B[2]**		
A25	T04	C14	O	PC Card Address 16-bit PC Card address lines. A25 is the most significant bit
A24	U02	B15		
A23	U01	C15		
A22	P04	C16		
A21	R02	A18		
A20	R01	C17		
A19	P01	B18		
A18	N02	A20		
A17	M04	C18		
A16	T01	A17		
A15	T02	A16		
A14	P02	B17		
A13	N03	A19		
A12	T03	D14		
A11	M01	D18		
A10	L01	E18		
A9	M03	B20		
A8	N01	B19		
A7	V01	A15		
A6	V02	A14		
A5	V03	B13		
A4	W02	A13		
A3	W03	C12		
A2	W04	A12		
A1	V04	B11		
A0	U05	C11		

[1] Terminal name for slot A is preceded with A_. For example, the full name for terminal T04 is A_A25.

[2] Terminal name for slot B s preceded with B_. For example, the full name for terminal C14 is B_A25.

Table 2-2 PCI1250 Terminal Functions

Name	No.		I/O Type	Function
D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	K03 J02 J04 H02 G01 W08 Y07 V07 J01 J03 H01 H03 G02 V08 W07 Y06	E19 E20 G18 G19 H18 B07 C08 A08 G17 F19 F20 F19 H19 A07 B08 D09	I/O	Card Data. 16-bit PC Card data lines. D15 is the most significant
16-Bit PC Card Interface Control Terminals (Slot A And Slot B)				
	Slot A[3]	**Slot B[4]**		
BVD1 (STSCHG/RI)	V06	A09		Battery Voltage Detect 1. Generated by 16-bit memory PC Cards that include batteries. BVD1 is used with BVD2 as an indication of the condition of the batteries on a memory PC Card. Both BVD1 and BVD2 are kept high when the battery is good. When BVD2 is low and BVD1 is high, the battery is weak and needs to be replaced. When BVD1 is low, the battery is no longer serviceable and the data in the memory PC Card is lost. See the *Card Status Change interrupt Configuration* register for enable bits. See the *Card Status Change* register and the *Interface Status* register for the status bits for this signal. Status Change (STSCHG). STSCHG is used to alert the system to a change in the READY, write protect, or battery voltage dead condition of a 16-bit I/O PC Card. Ring Indicate (RI). Ring indicate is used by 16-bit modem cards to indicate a ring detection.

[3] Terminal name for slot A is preceded with A_. For example, the full name for terminal W01 is A_ESET

[4] Terminal name for slot B s preceded with B_. For example, the full name for terminal B13 is B_RESET

Table 2-2 PCI1250 Terminal Functions

Name	No.		I/O Type	Function
BVD2 (SPKR)	Y05	D10	I	Battery Voltage Detect 2. Generated by 16-bit memory PC Cards that include batteries. BVD2 is used with BVD1 as an indication of the condition of the batteries on a memory PC Card. Both BVD1 and BVD2 are high when the battery is good. When BVD2 is low and BVD1 is high, the battery is weak and needs to be replaced. When BVD1 is low, the battery is no longer serviceable and the data in the memory PC Card is lost. See the Card Status Change Interrupt Configuration Register for enable bits. See the *Card Status Change* register and the I*nterface Status* register for the status bits for this signal. Speaker (SPKR) Speaker is an optional binary audio signal available only when the card and socket have been configured: for the 16-bit l/O interface. The audio signals from cards A and B are combined by the PCI 1250A and are output on the SPKROUT pin. DMA Request.: This pin may be used as the DMA request signal during DMA operations to a 16-bit PC Card that supports DMA. The PC Card asserts this signal to indicate a request for a DMA operation.
CD1 CD2	G03 W06	H20 C09	I	PC Card Detect 1 and Card Detect 2. CD1 and CD2 are connected to ground internally on the PC Card. When a PC Card is inserted into a socket. these signals are pulled low. The signal status is available by reading the interface status register
CE1 CE2	K01 L02	D20 D19	O	Card Enable 1 and Card Enable 2. These signals enable even and odd numbered address bytes. CE1 enables even numbered address bytes and CE2 enables odd numbered address bytes.
INPACK	Y01	D12	I	Input acknowledge. This signal is asserted by the PC Card when it can respond to an l/O read cycle at the current address. DMA Request. This pin may be used as the DMA request signal during DMA operations from a 16-bit PC Card that supports DMA. If used as a strobe, the PC Card asserts this signal to indicate a request for a DMA operation.
IORD	L04	E17	O	I/O read. IORD is asserted by the PCI1250A to enable 16-bit t/O PC Card data output during host l/O read cycles. DMA Write. This pin is used as the DMA write strobe during DMA operations from a 16-bit PC Card which supports DMA. The PCI1250A asserts this signal during DMA transfers from the PC Card to host memory.

Table 2-2 PCI1250 Terminal Functions

Name	No.		I/O Type	Function
IOWR	M02	C19	O	I/O Write IOWR is driven low by the PCI1250A to strobe write data into 16-bit l/O PC Cards during host l/O write cycles. DMA Read. This pin is used as the DMA write strobe during DMA operations from a 16-bit PC Card that supports DMA. The PCI1250A asserts this signal during transfers from host memory to the PC Card.
OE	L03	C20	O	Output Enable. OE is driven low by the PCl1250A to enable 16-bit Memory PC Card data output during host memory read cycles. DMA terminal count. This pin is used as TC during DMA operations to a 16-bit PC Card which supports DMA. The PCI1250A asserts this signal to indicate terminal count for a DMA write operation
READY/IREQ	Y04	A10	I	The ready function is provided by the READY signal when the 16-bit PC Card and the host socket are configured for the memory-only interface. READY is driven low by the 16-bit Memory PC Cards to indicate that the memory card circuits are busy processing a previous write command. READY is driven high when the 16-bit Memory PC Card is ready to accept a new data transfer command. Interrupt Request. IREQ is asserted by a 16-bit l/O PC Card to indicate to the host that a device on the 16-bit l/O PC Card requires service by the host software. IREQ is high (deasserted) when no interrupt is requested.
REG	Y02	B12	O	Attribute memory select. REG remains high for all common memory accesses. When REG is asserted access is limited to attribute memory (OE or WE active) and to 1he l/O space (IORD or IOWR active}. Attribute memory is a separately accessed section of card memory and is generally use to record card capacity and other configuration and attribute information. DMA acknowledge. This pin is used as a DACK during DMA operations to a 16-bit PC Card that supports DMA. The PCI1250A asserts this signal to indicate a DMA operation. This signal is used in conjunction with the DMA read (IOWR) or DMA write (IORD) strobes to transfer data.
RESET	W01	C13	O	PC Card reset. RESET forces a hard reset to a 16-bit PC Card
WAIT	V05	B10	I	Bus cycle wait. WAIT is driven by a 16-bit PC Card to delay the completion of (i.e.. extend) the memory or l/O cycle that is in progress.

Table 2-2 PCI1250 Terminal Functions

Name	No.		I/O Type	Function
WE	P03	D16	O	Write enable. WE is used to strobe memory write data into 16-bit memory PC Cards. WE is also use for memory PC Cards that employ programmable memory technologies. DMA terminal count. This pin is used as TC during DMA operations to a 16-bit PC Card which supports DMA. The PC1031 asserts this signal to indicate terminal count for a DMA read operation.
WP (IOIS16)	U07	B09	I	Write protect. This signal applies to 16-bit memory PC Cards. WP reflects the status of the write-protect switch on 16-bit memory PC Cards. For 16-bit I/O cards, WP is used for the 16-bit port (IOSI16) function. IOIS16 (I/O is 16-bits). This signal applies to 16-bit I/O PC Cards. IOIS16 is asserted by the 16-bit PC Card when the address on the bus corresponds to an address to which the 16-bit PC Card responds and the I/O port that is addressed is capable of 16-bit accesses. DMA request. This pin can be used as the DMA request signal during DMA operations to a 16-bit PC Card which supports DMA. If used, the PC Card asserts this signal to indicate a request for a DMA operation
VS1 VS2	Y03 U03	A11 B14	I/O	Voltage Sense 1 and Voltage Sense 2. VS1 and VS2, when used in conjunction with each other, determine the operating voltage of the 16-bit PC Card.
Cardbus PC Card Interface System Terminals				
	Slot A[5]	**Slot B[6]**		
CCLK	T01	A17	O	CardBus PC Card Clock. This signal provides synchronous timing for all transactions on the] CardBus interface. All signals except CRST, CCLKRUN, CINT, CSTSCHG. CAUDIO, CCD2:1, and CVS2.1 are sampled on the rising edge of the CCLK, and all timing parameters are defined with the rising edge of this signal. The CardBus clock operates at the PCI bus clock frequency, but it can be stopped in the low state or slowed down for power savings.

[5] Terminal name for slot A is preceded with A_. For example, the full name for terminal N03 is A_CPAR.

[6] Terminal name for slot B s preceded with B_. For example, the full name for terminal A19 is B_CPAR.

Table 2-2 PCI1250 Terminal Functions

Name	No.		I/O Type	Function
CRSST	W01	C13	I/O	CardBus PC Card Reset. This signal is used to bring CardBus PC Card specific registers, sequencers, and signals to a known state. When CRST is asserted, all CardBus PC Card signals must be 3-statedt and the PCI1250A will drive these signals to a valid logic level. Assertion may be asynchronous to the CCLK. But deassertion must be synchronous to the CCLK.
CCLKRUN	U07	B09	O	CardBus PC Card Clock Run. This signal is used by a CardBus PC Card to request an increase in the CCLK frequency. and the PCI 1 250A to indicate that the CCLK frequency will be decreased.
CardBus PC Card Address and Data Terminals (Slot A and Slot B)				
CAD31 CAD30 CAD29 CAD28 CAD27 CAD26 CAD25 CAD24 CAD23 CAD22 C AD21 CAD20 CAD19 CAD18 CAD17 CAD16 CAD15 CAD14 CAD13 CAD12 CAD11 CAD10 CAD9 CAD8 CAD7 CAD6 CAD5 CAD4 CAD3 CAD2 CAD1 CAD0	W08 Y07 W07 V07 Y06 U05 V04 W04 W03 W02 V03 V02 T04 V01 U02 M04 M02 M03 L04 M01 L03 L02 L01 K03 J01 J04 J03 H02 H01 G01 H03 G02	B07 C08 B08 A08 D09 C11 B11 A12 C12 A13 B13 A14 C14 A15 B15 C18 C19 B20 E17 D18 C20 D19 E18 E19 G17 G18 F19 G19 F20 H18 G20 H19	I/O	PC Card Address and Data bus. These signals make up the multiplexed CardBus address and data bus on the CardBus interface. During the address phase of a CardBus cycle, CAD31:0 contain a 32-bit address. During the data phase of a CardBus cycle, CAD31:0 contain data. CAD31 is the most significant bit

Table 2-2 PCI1250 Terminal Functions

Name	No.		I/O Type	Function
CC/BE3 CC/BE2 CC/BE1 CC/BE0	Y02 T03 N01 K01	B12 D14 B19 D20	I/O	CardBus Bus Commands and Byte Enables. The command and byte enable signals are multiplexed on the same CardBus terminals. During the address phase of a CardBus cycle, CC/BE3:0 defines the bus command. During the data phase, this four-bit bus is used as byte enables. The byte enables determine which byte paths of the full 32-bit data bus carry meaningful data. CC/BE0 applies to byte 0 (CAD7:0), CC/BE1 applies to byte 1 (CAD15:8), CC/BE2 applies to byte 2 (CAD23:8), and CC/BE3 applies to byte 4(CAD31:24)
CPAR	N03	A19	I/O	CardBus Parity. In all CardBus read and write cycles, the PCI1250A calculates even parity cross the CAD and CC/BE buses. As an initiator during CardBus cycles, the PC11250A outputs this parity indicator with a one CCLK delay. As a target during CardBus cycles, the calculated parity is compared to the initiator's parity indicator; a miscompare can result in a parity error assertion.
Cardbus Interface Control Terminals				
	Slot A	**Slot B**		
CAUDIO	Y05	D10	I	CardBus Audio. This signal is a digital input signal from a PC Card to the system speaker. The PCI1250A supports the binary audio mode, and outputs a binary signal from the card to the SPKROUT signal
CBLOCK	P01	B18	I/O	CardBus Lock. This signal is used to gain exclusive access to a target
CCD1 CCD2	G03 W06	H20 C09	I	CardBus Detect 1 and CardBus Detect 2. These signals are used in conjunction with voltage sense signals to identify ca d insertion and interrogate cards to determine the operating voltage and card type.
CDEVSEL	R02	A18	I/O	CardBus device select. The PCI1250A asserts this signal to claim a CardBus cycle as the target device. As a CardBus initiator on the bus, the PCI1250A monitors this signal until a target responds. If no target responds before time-out occurs, then the PCI1250A will terminate the cycle with an initiator abort.
CFRAME	U01	C15	I/O	CardBus cycle frame. This signal is driven by the initiator of a CardBus bus cycle. CFRAME is asserted to indicate that a bus transaction is beginning. and data transfers continue while this signal is asserted. When CFRAME is deasserted the CardBus bus transaction is in the final data phase.
CGNT	P03	D16	I	CardBus bus grant. This signal is driven by the PCI1250A to grant a CardBus PC Card access to the CardBus bus after ihe current data transaction has completed.

Table 2-2 PCI1250 Terminal Functions

Name	No.		I/O Type	Function
CINT	Y04	A10	I	CardBus interrupt. This signal is asserted low by a CardBus PC Card to request interrupt servicing from the host.
CIRDY	T02	A16	I/O	CardBus initiator ready. CIRDY indicates the CardBus initiator's ability to complete the current data phase of the transaction. A data phase is completed upon a rising edge of CCLK where both CIRDY and CTRDY are asserted. Until CIRDY and CTRDY are both sampled asserted, wait states are inserted.
CPERR	P02	B17	I/O	CardBus Parity Error. This signal is used to report parity errors during CardBus transactions, except during special cycles. It is driven low by a target two clocks following that data when a parity error is detected.
CREQ	Y01	D12	I	CardBus Request. This signal indicates to the arbiter that the CardBus PC Card desires use of the CardBus bus as an initiator
CSERR	V05	B10	I	CardBus System Error. This signal reports address parity errors and other system errors which could lead to catastrophic results. CSERR is driven by the card synchronous to CCLK but ceasserted by a weak pull-up, and may take a few CCLK periods. The PCI1250A can report CSERR to the system by assertion of SERR on the PCI interface.
CSTOP	R01	C17	I/O	CardBus Stop Signal. This signal is driven by a CardBus target to request the initiator to stop the current CardBus transaction. This signal is used for target disconnects, and is commonly asserted by target devices which do not support burst data transfers.
CSTSCHG	V06	A09	I	CardBus Status Change. CSTSCHG is used to alert the system to a change in the card's status, and is used as a wake-up mechanism.
CTRDY	P04	C16	I/O	CardBus Target Ready. CTRDY indicates the CardBus target's ability to complete the current data phase of the transaction. A data phase is completed upon a rising edge of CCLK where both CIRDY and CTRDY are asserted; until which wait states are inserted
CVS1 CVS2	Y03 U03	A11 B14	I/O	CardBus Voltage Sense 1 and Voltage Sense 2. These signals are used in conjunction with card detect signals to identify card insertion and interrogate cards to determine the operating voltage and card type.

Table 2-2 PCI1250 Terminal Functions

Name	No.	I/O Type	Function
System Interrupt Terminals			
GPIO3/INTA	V13	I/O	GPI03/INTA Parallel PCI Interrupt. This terminal can be connected to an available PCI interrupt if parallel PCI interrupts are used, and the PCI1250A will output PCI INTA through this terminal. Refer to the Interrupt Subsystem description in this document for details on interrupt signaling. This terminal defaults to a general purpose input
IRQSER/INTB	W13	I/O	IRQSER Serial Interrupt Signal / INTB Parallel PCI Interrupt. When this terminal is configured as IRQSER, it provides the IRQSER style serial interrupting scheme. Serialized PCI interrupts can also be sent in the IRQSER stream. This terminals can be configured as the parallel PCI INTB interrupt. Refer to the Interrupt Subsystem description in this document for details on interrupt signaling. This terminal defaults to the IRQSER signal since this is the default interrupt signaling method
IRQMUX7 IRQMUX6 IRQMUX5 IRQMUX4 IRQMUX3 IRQMUX2 IRQMUX1 IRQMUX0	Y12 U11 W10 Y09 W09 V09 U09 Y08	O	The primary function of these terminals is to provide the ISA type IRQ signaling supported by the PCI1250A. These Interrupt mux outputs can be mapped to any of 15 IRQs. The Device Control register must be programmed for the ISA IRQ interrupt mode and the IRQMUX Routing Register must have the IRQ routing programmed before these terminals are enabled. All of these terminals have secondary functions, such as PC/PCI DMA request/grant, ring indicate output, and zoom video status. that can be selected; with the appropriate programming of this register. When the secondary functions are enabled, the respective terminals are not available for IRQ routing. See the IRQMUX Routing register for programming options
RI-OUT/PME	Y13	O	Ring indicate Output/Power Management Event. RI_OUT allows the RI input from one of the PC Cards to pass through o the system. This pin is the RI_OUT signal when the PCI1250A is in the D0 (fully on) state and provides the PME signal when the device is in a D1, D2, or D3 state. IRQMUX4 or IRQMUX3 can be used to route the RI_OUT signal when the PME signal is routed on pin Y13 and a PC Card requires a ring indicate signal
PC Card Power Switch Terminals			
LATCH	W13	O	3-Line power Switch latch. This signal is asserted by the PCI1250A to indicate to the PC Card power switch that the data on the DATA line is valid.

Table 2-2 PCI1250 Terminal Functions

Name	No.		I/O Type	Function
CLOCK	U12		I/O	3-Line Power Switch Clock. Information on the DATA line is sampled at the rising edge of CLOCK. This terminal defaults to an input, but can be changed to a PCI1250A output by using the P2CCLK bit in the I/O System Control Register. The TPS2206 defines the maximum frequency of this signal to be 2MHz. If a system design defines this terminal an output, then this terminal requires an external pull-up resister. The frequency of the PCI1250A output CLOCK is derived from dividing the PCI CLK by 36
DATA	V12		O	3-Line Power Switch Data. This signal is used to serially communicate socket power control information to the power switch.
Zoomed Video Terminals				
		I/O and Memory Interface Signal		
ZV_HREF	A06	A10	O	Horizontal Sync to the zoom video port.
ZV_VSYNC	C07	A11	O	Vertical sync to the zoom video port.
ZV_Y7 ZV_Y6 ZV_Y5 ZV_Y4 ZV_Y3 ZV_Y2 ZV_Y1 ZV_Y0	A03 B04 C05 B05 C06 D07 A05 B06	A20 A14 A19 A13 A18 A8 A17 A9	O	Video data to the zoom video port in YV:4:2:2 format.
D02 C03 B01 B02 A02 C04 B03 D05	D02 C03 B01 B02 A02 C04 B03 D05	A25 A12 A24 A15 A23 A16 A22 A21	O	Video data to the zoom video port in YV:4:2:2 format.
ZV_SCLK	C02	A7	O	Audio SCLK PCM signal.
ZV_MCLK	D03	A6	O	Audio MCLK PCM signal.
ZV_PCLK	E01	IOIS16	O	Pixel clock (PCLK) to the zoom video port.
ZV_LRCLK	E03	INPACK	O	Audio LRCLK PCM signal.
ZV_SDATA	E02	SPKR	O	Audio PCM data signal (SDATA)
ZV_RSVD	F1 F2 F3 G4		O	Reserved. No connection.
ZV_RSV1 ZV_RSV0	C1 E4	A5 A4	O	Reserved. No connection in PC Card. These signals are put into a high-impedance state by the host adapter.

Table 2-2 PCI1250 Terminal Functions

Name	No.	I/O Type	Function
PC/PCI DMA Terminals			
PCREQ/ IRQMUX7	Y12	O	PC/PCI DMA Request. This signal is used to request DMA transfers as DREQ in a system supporting the PC. PCI DMA scheme. IRQMUX7. When this terminal is configured for IRQMUX7, it provides the IRQMUX7 interrupt output of the interrupt mux, and can be mapped to any of 15 ISA type IRQs. The IRQMUX7 signal takes precedence over PCREQ, and should not be enabled in a system using PC/PCI DMA. This pin is also used for the serial EEPROM interface.
PCGNT/ IRQMUX6	U11	I/O	PC/PCI DMA Grant. This signal is used to grant the DMA channel to a requester in a system supporting the pr PCI DMA scheme. IRQMUX6. When :his terminal is configured for IRQMUX6, it provides the IRQMUX6 interrupt output of the interrupt mux, and can be mapped to any of 15 ISA type IRQs. The IRQMUX6 signal takes precedence over PCGNT, and should not be enabled in a system using PC/PCI DMA. This pin is also used for the serial EEPROM interface.
Miscellaneous Terminals			
GPIO0/ LEDA1	V11	I/O	GPIO0 / Socket Activity LED Indicator 1. When this signal is configured as LEDA1 it provides an output indicating PC Card socket O activity. Otherwise, this signal can be configured as a general purpose input and output, GPIO0. The zoom video enable signal (ZVSTAT) can also be routed to this signal through the GPIO0 Control register. This terminal defaults to a general purpose input.
GPIO1/ LEDA2	W11	I/O	GPI01 / Socket Activity LED Indicator 2. When this signal is configured as LEDA2 it provides an output indicating PC Card socket 1 activity. Otherwise, this signal can be configured as a general purpose input and output. GPIO1. A CSC interrupt can be generated on a GPDATA change, and this input can be used for power switch overcurrent (OC) sensing. Refer to the GPI01 Control resister for programming details. This terminal defaults to a general purpose input.
SUSPEND	Y1	I	Suspend. This signal is used to protect the internal registers from clearing when the PRST signal is asserted. For details on implementing SUSPEND in your system power management scheme refer to the section on SUSPEND mode.

Table 2-2 PCI1250 Terminal Functions

Name	No.	I/O Type	Function
SPKROUT	Y10	O	Speaker Output. This signal is the output to the host system that can carry the SPKR or CAUDIO signal through the PCI1250A from the PC Card interface. This signal is driven as the exclusive OR combination of card SPKR//CAUDIO inputs.

2.2 Aladdin IV (M1531/M1533)

The Aladdin-IV is the succeeding generation chipset of Aladdin-III from Acer Labs. It maintains the best system architecture (two-chip solution) to achieve the best system performance with the lowest system cost (TTL-free). The Aladdin-IV consists of two BGA chips to give the 586-class system a complete solution with most up-to-date features and architecture for multimedia/ multithreading OS and software applications. It utilizes the modern BGA package to improve the AC characterization, resolves system bottleneck and makes the system manufacturing easier.

2.2.1 M1531

The M1531 includes:

- Higher CPU bus frequency (up to 83.3 MHz) interface for the incoming Cyrix M2 and AMD K6, PBSRAM and Memory Cache L2 controller
- Internal MESI tag bits (8K x 2) to reduce cost and enhance performance
- High-performance FPM/EDO/SDRAM DRAM controller
- PCI 2.1 compliant bus interface
- Smart deep buffer design for CPU-to-DRAM, CPU-to-PCI, and PCI-to-DRAM to achieve the best system performance
- Highly efficient PCI fair arbiter
- The most flexible 32/64-bit memory bus interface for the best DRAM upgrade ability and ECC/parity design to enhance the system reliability

With the concurrent bus design, PCI-to-PCI access can run concurrently with CPU-to-L2 and CPU-to-DRAM access, while PCI-to-DRAM access can run concurrently with CPU-to-L2 access. The M1531 also supports the snoop ahead feature to achieve the PCI master full-bandwidth access (133 MB) and provides the enhanced power management features including ACPI support, suspend DRAM refresh, and internal chip power control to support the Microsoft's On Now technology OS.

The M1533 offers the best power management system solution. It integrates ACPI support, deep green function, two-channel dedicated Ultra-33 IDE master controller, two-port USB controller, SMBus controller, and PS2 keyboard/mouse controller.

The M1543 provides the best desktop system solution. It integrates ACPI support, green function, two-channel dedicated Ultra-33 IDE Master controller, two-port USB controller, SMBus controller, PS/2 keyboard/mouse controller and the Super I/O (Floppy Disk Controller, two serial port/one parallel port) support.

The Aladdin-IV gives a highly-integrated system solution and a most up-to-date architecture to provide the best cost/performance system solution for desktop and notebook vendors.

2.2.1.1 Features

- Supports all Intel/Cyrix/AMD/TI/IBM 586 processors. Host bus at 83.3, 75, 66, 60 and 50 MHz at 3.3V/2.5V
- Supports Linear Wrap mode for Cyrix M1 and M2
  - Write-Allocation feature for K6
  - Pseudo-Synchronous PCI bus access
    (CPU bus: 75 MHz - PCI bus: 30 MHz, CPU bus: 83.3 MHz - PCI bus: 33 MHz)
- Supports Pipelined-burst SRAM/Memory Cache
  - Direct mapped, 256 KB/512 KB/1 MB
  - Write-Back/Dynamic-Write-Back cache policy
  - Built-in 8K x 2 bit SRAM for MESI protocol to reduce cost and enhance performance
  - Cacheable memory up to 64 MB with 8-bit Tag SRAM
  - Cacheable memory up to 512 MB with 11-bit Tag SRAM
  - 3-1-1-1-1-1-1-1 for Pipelined-burst SRAM/Memory Cache at back-to-back burst read and write cycles
  - 3.3V/5V SRAMs for Tag address
  - CPU single-read cycle L2 allocation
- Supports FPM/EDO/SDRAM DRAMs
  - 8 RAS lines up to 1 GB support
  - 64-bit data path to memory
  - Symmetrical/Asymmetrical DRAMs
  - 3.3V or 5V DRAMs
  - Duplicated MA[1:0] driving pins for burst access
  - No buffer needed for RASJ and CASJ and MA[1:0]
  - CBR and RAS-only refresh for FPM
  - CBR and RAS-only refresh and Extended refresh and self refresh for EDO
  - CBR and Self refresh for SDRAM
  - 16 Qword deep merging buffer for 3-1-1-1-1-1-1-1 posted-write cycle to enhance high-speed CPU burst access
  - 6-3-3-3-3-3-3-3 for back-to-back FPM read page hit, 5-2-2-2-2-2-2-2 for back-to-back EDO read page hit, 6-1-1-1-2-1-1-1 for back-to-back SDRAM read page hit, 2-2-2-2 for retired data for posted write on FPM and EDO page-hit, x-1-1-1 for retired data for posted write SDRAM page-hit
  - Enhanced DRAM page miss performance
  - Supports 64 Mbit (16M x 4, 8M x 8, 4M x 16) technology of DRAMs
  - Supports Programmable-strength RAS/CAS/ MWEJ/MA buffers
  - Supports Error Checking and Correction (ECC) and Parity for DRAM

- Supports the most flexible six 32-bit populated banks of DRAM for easy DRAM upgrade
- Supports SIMM and DIMM
- Synchronous/Pseudo Synchronous 25/30/33MHz 3.3V/5V tolerance PCI interface
- Concurrent PCI architecture
- PCI bus arbiter: five PCI masters and M1533/ M1543 (ISA Bridge) supported
- 6 DWords for CPU-to-PCI memory write posted buffers
- Converts back-to-back CPU to PCI memory write to PCI burst cycle
- 38/22 Dwords for PCI-to-DRAM Write-posted/ Read-prefetching buffers
- PCI-to-DRAM up to 133 MB/sec bandwidth (even when L1/L2 write-back)
- L1/L2 pipelined-snoop ahead for PCI-to-DRAM cycle
- Supports PCI mechanism #1 only
- Complies with PCI spec. 2.1 (N(32/16/8)+8 rule, passive release, fair arbitration)
- Enhanced performance for Memory-Read-Line, Memory-Read-Multiple and Memory-write-Invalidate PCI commands

- Enhanced Power Management
  - ACPI support
  - PCI bus CLKRUN function
  - Dynamic Clock Stop
  - Power-on Suspend
  - Suspend to Disk
  - Suspend to DRAM
  - Self refresh during Suspend
- 328-pin (27mm x 27mm) BGA package

2.2.1.2 Pin Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	NC	PHLDAJ	AD3	AD6	AD8	AD12	PAR	TRDYJ	AD17	AD22	AD25	AD30	REQJ3	GNTJ2	GNTJ3	MPD2	MPD0	MD61	MD29	MD62
B	BEJ0	PHLDJ	AD2	AD5	AD7	AD11	CBEJ1	DEVSELJ	AD16	AD21	AD24	AD29	REQJ2	GNTJ1	MPD5	MPD1	MD63	MD27	MD60	MD28
C	BEJ3	BEJ2	BEJ1	AD4	CBEJ0	AD10	AD15	STOPJ	CBEJ2	AD20	CBEJ3	AD28	REQJ1	GNT0J	MPD4	MD30	MD25	MD58	MD26	MD59
D	BEJ6	BEJ5	BEJ4	AD0	AD1	AD9	AD14	LOCKJ	FRAMEJ	AD19	AD23	AD27	REQJ0	MPD7	MPD3	MD55	MD23	MD56	MD24	MD57
E	DCJ	HITMJ	EADSJ	BEJ7	RSTJ	PCIMRQJ	AD13	SERRJ	IRDYJ	AD18	PCLKIN	AD26	AD31	MPD6	MD31	MD20	MD53	MD21	MD54	MD22
F	BRDYJ	BOFFJ	SMIACTJ	HLOCKJ	ADSJ	VCC_B								VCC_C	VCC_C	MD50	MD18	MD51	MD19	MD52
G	HD63	CACHEJ	AHOLD	KENJ	NAJ	VCC_A			**M1531**						VCC_C	MD15	MD48	MD16	MD49	MD17
H	HD60	HD61	HD62	WRJ	MIOJ			GND	GND	GND	GND	GND	GND			MD45	MD13	MD46	MD14	MD47
J	HD55	HD56	HD57	HD58	HD59			GND	GND	GND	GND	GND	GND			MD10	MD43	MD11	MD44	MD12
K	HD51	HD52	HD53	HD54	HCLKIN			GND	GND	GND	GND	GND	GND			MD40	MD8	MD41	MD9	MD42
L	HD46	HD47	HD48	HD49	HD50			GND	GND	GND	GND	GND	GND			MD5	MD38	MD6	MD39	MD7
M	HD41	HD42	HD43	HD44	HD45			GND	GND	GND	GND	GND	GND			MD35	MD3	MD36	MD4	MD37
N	HD36	HD37	HD38	HD39	HD40			GND	GND	GND	GND	GND	GND		VDD5S	REQJ4	GNTJ4	MD1	MD34	MD2
P	HD31	HD32	HD33	HD34	HD35	VCC_A									VCC_C	32K	SUSPEND	MD32	MD0	MD33
R	HD26	HD27	HD28	HD29	HD30	VDD5	VCC_A							VCC_B	VCC_C	RASJ6	RASJ7	CASJ2	CASJ7	CASJ3
T	HD21	HD22	HD23	HD24	HD25	HD0	A12	A5	GWEJ	COEJ	CADVJ	TWEJ	MAA0	MAA1	TIO8	TIO9	TIO10	RASJ1	RASJ0	CASJ6
U	HD16	HD17	HD18	HD19	HD20	HD1	A13	A8	CCSJ	BWEJ	CADSJ	TIO0	TIO1	MAB0	MAB1	MA5	MWEJ	RASJ4	RASJ3	RASJ2
V	HD15	HD14	HD13	HD6	HD3	A17	A14	A10	A4	A29	A25	A24	A23	TIO2	MA2	MA4	MA8	CASJ5	CASJ1	RASJ5
W	HD12	HD11	HD10	HD5	HD2	A18	A15	A11	A7	A30	A31	A22	A21	TIO4	TIO6	MA3	MA7	MA10	CASJ0	CASJ4
Y	HD9	HD8	HD7	HD4	A20	A19	A16	A9	A6	A3	A28	A26	A27	TIO3	TIO5	TIO7	MA6	MA9	MA11	NC

Figure 2-2 M1531 Pin Diagram (Top View)

2.2.1.3 Signal Descriptions

Table 2-3 M1531 Signal Descriptions

Signal	Type	Description
Host Interface 3.3V/2.5V		
A[31:3]	I/O Group A	Host Address Bus Lines. A[31:3] have two functions. As inputs, along with the byte enable signals, these pins serve as the address lines of the host address bus which define the physical area of memory or I/O being accessed. As outputs, the M1531 drives them during inquiry cycles on behalf of PCI masters.
BEJ[7:0]	I Group A	Byte Enables. These are the byte enable signals for the data bus. BEJ[7] applies to the most significant byte and BEJ[0] applies to the least significant byte. They determine which byte of data must be written to the memory, or are requested by the CPU. In local memory read and line-fill cycles, these inputs are ignored by the M1531.
ADSJ	I Group A	Address Strobe. The CPU will start a new cycle by asserting ADSJ first. The M1531 will not precede to execute a cycle until it detects ADSJ active.
BRDYJ	O Group A	Burst Ready. The assertion of BRDYJ means the current transaction is complete. The CPU terminates the cycle by receiving 1 or 4 active BRDYJs depending on different types of cycles.
NAJ	O Group A	Next Address. This signal is asserted by the M1531 to inform the CPU that pipelined cycles are ready for execution.
AHOLD	O Group A	CPU AHold Request Output. It connects to the input of CPU's AHOLD pin and is actively driven for inquiry cycles.
EADSJ	O Group A	External Address Strobe. This signal is connected to the CPU EADSJ pin. During PCI cycles, the M1531 asserts this signal to proceed snooping.
BOFFJ	O Group A	CPU Back-Off. If BOFFJ is sampled active, CPU will float all its buses in the next clock. M1531 asserts this signal to request CPU floating all its output buses.
HITMJ	I Group A	Primary Cache Hit and Modified. When snooped, the CPU asserts HITMJ to indicate that a hit to a modified line in the data cache occurred. It is used to prohibit another bus master from accessing the data of this modified line in the memory until the line is completely written back.
MIOJ	I Group A	Host Memory or I/O. This bus definition pin indicates the current bus cycle is either memory or input/ output.
DCJ	I Group A	Host Data or Code. This bus definition pin is used to distinguish data access cycles from code access cycles.
WRJ	I Group A	Host Write or Read. When WRJ is driven high, it indicates the current cycle is a write. Inversely, if WRJ is driven low, a read cycle is performed.
HLOCKJ	I Group A	Host Lock. When HLOCKJ is asserted by the CPU, the M1531 will recognize the CPU is locking the current cycles.
CACHEJ	I Group A	Host Cacheable. This pin is used by the CPU to indicate the system that CPU wants to perform a line fill cycle or a burst write back cycle. If it is driven inactive in a read cycle, the CPU will not cache the returned data, regardless of the state of KENJ.

Table 2-3 M1531 Signal Descriptions

Signal	Type	Description
KENJ/INV	O Group A	Cache Enable Output. This signal is connected to the CPU's KENJ and INV pins. KENJ is used to notify the CPU whether the address of the current transaction is cacheable. INV is used during L1 snoop cycles. The M1531 drives this signal high (low) during the EADSJ assertion of a PCI master write (read) snoop cycle.
SMIACTJ	I Group A	SMM Interrupt Active. This signal is asserted by the CPU to inform the M1531 that SMM mode is being entered.
HD[63:0]	I/O Group A	Host Data Bus Lines. These signals are connected to the CPU's data bus. HD[63] applies to the most significant bit and HD[0] applies to the least significant bit.
MPD[7:0]	I/O Group C	DRAM Parity /ECC check bits. These are the 8 bits for parities/ECC check bits over DRAM data bus. MPD[7] applies to the most significant bit and MPD[0] applies to the least significant bit.
RASJ[7] / SRASJ[0]	O Group C	Row Address Strobe 7, (FPM/EDO) of DRAM row 7. SDRAM Row Address Strobe (SDRAM) copy 0. It connects to SDRAM RASJ. This is a multifunction pin and determined by Index-5Ch bit0.
RASJ[6] / SCASJ[0]	O Group C	Row Address Strobe 6, (FPM/EDO) of DRAM row 6. SDRAM Column address strobe (SDRAM) copy 0. It connects to SDRAM CASJ. This is a multifunction pin and determined by Index-5Ch bit0.
RASJ[5:0]	O Group C	Row Address Strobes. These signals are used to drive the corresponding RASJs of FPM/EDO DRAMs. In SDRAM, they are used to drive the corresponding SDRAM CSJs.
CASJ[7:0] / DQM[7:0]	O Group C	Column Address Strobes or Synchronous DRAM Input/Output Data Mask. These CAS signals should be connected to the corresponding CASJs of each bank of DRAM. The value of CASJs equals that of HBEJs for write cycles. During DRAM read cycles, all of CASJs will be active. In SDRAM, these pins act as synchronized output enables during a read cycle and the byte mask during write cycle, these pins are connected to SDRAM DQM[7:0].
MA[11:2]	O Group C	DRAM Address Lines. These signals are the address lines[11:2] of all DRAMs. The M1531 supports DRAM types ranging from 256K to 64Mbits.
MAA[1:0]	O Group C	Memory Address copy A for [1:0]. These signals are the address lines[1:0] copy 0 of all DRAMs.
MAB[1:0]	O Group C	Memory Address copy B for [1:0]. These signals are the address lines[1:0] copy 1 of all DRAMs.
MWEJ[0]	O Group C	DRAM Write Enable. This is the DRAM write enable pin and behaves according to the early-write mechanism, i.e. , it activates before the CASJs do. For refresh cycles, it will remain deasserted.
MD[63:0]	I/O Group C	Memory Data. These pins are connected to DRAM's data bits. MD[63] applies to the most significant bit and MD[0] applies to the least significant bit.
CLKEN[0]/ REQJ[4]	I/O Group C	SDRAM Clock Enable Copy 0 or PCI Master Request. This signal is used as SDRAM clock enable copy 0 to do self refresh during suspend. It can also be used as bus request signal of the fifth PCI master. This function is controlled by Index -5Dh bit 1.

Table 2-3 M1531 Signal Descriptions

Signal	Type	Description
CLKEN[1]/ GNTJ[4]	O Group C	SDRAM Clock Enable Copy 1 or PCI Master Grant. This signal is used as SDRAM clock enable copy 1 to do self refresh during suspend. It can also be used as grant signal of the fifth PCI master. This function is controlled by Index -5Dh bit 1.
Secondary Cache Interface 3.3V/2.5V Tolerance		
CADVJ	O Group A	Synchronous SRAM Advance. This signal will make PBSRAM/Memory Cache internal burst address counter advance.
CADSJ	O Group A	Synchronous SRAM Address Strobe. This signal connects to PBSRAM/ Memory Cache ADSCJ.
CCSJ	O Group A	Synchronous SRAM Chip Select. This signal connects to PBSRAM/Memory Cache CE1J to mask ADSPJ and enable ADSCJ sampling.
GWEJ	O Group A	Synchronous SRAM Global Write Enable. This signal will write all the byte lanes data into PBSRAM/Memory Cache.
COEJ	O Group A	Synchronous SRAM Output Enable. This signal will enable the data output driving of PBSRAM/Memory Cache.
BWEJ	O Group A	Synchronous SRAM Byte-Write Enable. This signal connects to byte write enable of PBSRAM/Memory Cache.
TIO[10]/ MWEJ[1]/ MKREFRQJ	I/O Group C	SRAM Tag[10] or another copy of MWEJ or DRAM Cache MKREFRQJ. This pin is used for multifunction. It can be SRAM tag address bit 10, or another copy of MWEJ connected to DRAM, or MKREFRQJ connected to DRAM Cache. Refer to Register Index-41h bit 6, bit3 and bit0 description.
TIO[9]/ SRASJ[1]	I/O Group C	SRAM Tag[9] or Synchronous DRAM (SDRAM) RAS copy 1. This pin is used for multifunction. It can be SRAM tag address bit 9, or another copy of SRASJ connected to SDRAM. Refer to Register Index-41h bit3 and bit0 description.
TIO[8]/ SCASJ[1]	I/O Group C	SRAM Tag[8] or Synchronous DRAM (SDRAM) CAS copy 1. This pin is used for multifunction. It can be SRAM tag address bit 8, or another copy of SCASJ connected to SDRAM. Refer to Register Index-41h bit3 and bit0 description.
TIO[7:0]	I/O Group B	SRAM Tag[7:0]. This pin contains the L2 tag address for 256-KB L2 caches. TIO[6:0] contain the L2 tag address and TIO7 contains the L2 cache valid bit for 512-KB caches. TIO[5:0] contain L2 tag address, TIO7 contains L2 cache valid bit and TIO6 contains the L2 cache dirty bit for 1-MB cache. Refer to index-41h cache configuration table.
TAGWEJ	O Group B	Tag Write Enable. This signal, when asserted, will write into the external tag new state and tag addresses.
PCI Interface 3.3V/2.5V Tolerance		
AD[31:0]	I/O Group B	PCI Address and Data Bus Lines. These lines are connected to the PCI bus. AD[31:0] contain the information of address or data for PCI transactions.
CBEJ[3:0]	I/O Group B	PCI Bus Command and Byte Enables. Bus commands and byte enables are multiplexed in these lines for address and data phases, respectively.
FRAMEJ	I/O Group B	Cycle Frame of PCI Buses. This indicates the beginning and duration of a PCI access. It will be as an output driven by M1531 on behalf of CPU, or as an input during PCI master access.

Table 2-3 M1531 Signal Descriptions

Signal	Type	Description
DEVSELJ	I/O Group B	Device Select. When the target device has decoded the address as its own cycle, it will assert DEVSELJ.
IRDYJ	I/O Group B	Initiator Ready. This signal indicates the initiator is ready to complete the current data phase of transaction.
TRDYJ	I/O Group B	Target Ready. This pin indicates the target is ready to complete the current data phase of transaction.
STOPJ	I/O Group B	Stop. This signal indicates the target is requesting the master to stop the current transaction.
LOCKJ	I/O Group B	Lock Resource Signal. This pin indicates the PCI master or the bridge intends to do exclusive transfers.
REQJ[3:0]	I Group B	Bus Request signals of PCI Masters. When asserted, it means the PCI Master is requesting the PCI bus ownership from the arbiter.
GNTJ[3:0]	O Group B	Grant signals to PCI Masters. When asserted by the arbiter, it means the PCI master has been legally granted to own the PCI bus.
PHLDJ	I Group B	PCI bus Hold Request. This active low signal is a request from M1533/M1543 for the PCI bus.
PHLDAJ	O Group B	PCI bus Hold Acknowledge. This active low signal grants PCI bus to M1533/M1543.
PAR	I/O Group B	Parity bit of PCI bus. It is the even parity bit across PAD[31:0] and CBEJ[3:0].
SERRJ/ CLKRUNJ	I/O Group B	System Error or PCI Clock RUN. If the M1531 detects parity errors in DRAMs, it will assert SERRJ to notify the system. As CLKRUNJ, this signal will connect to M1533 CLKRUNJ to start, or maintain the PCI CLOCK. It is a multifunction pin and determined by Index-77h bit0.
Clock, Reset, and Suspend		
HCLKIN	I Group A	CPU bus Clock Input. This signal is used by all of the M1531 logic that is in the Host clock domain.
RSTJ	I Group B	System Reset. This pin, when asserted, resets the M1531 state machine, and sets the register bits to their default values.
Clock, Reset, and Suspend		
PCICLK	I Group B	PCI bus Clock Input. This signal is used by all of the M1531 logic that is in the PCI clock domain.
PCIMRQJ	O Group B	Total PCI Request. This signal is used to notify M1533/M1543 that there is PCI master requesting PCI bus.
SUSPENDJ	I Group C	Suspend. When actively sampled, the M1531 will enter the I/O suspend mode. This signal should be pulled high when the suspend feature is disabled.
OSC32KO	I Group C	The refresh reference clock of frequency 32 KHz during suspend mode. This signal should be pulled to a fixed value when the suspend feature is disabled.

Table 2-3 M1531 Signal Descriptions

Signal	Type	Description
Power Pins		
VCC_A	P	Vcc 3.3V or 2.5V Power for Group A. This power is used for CPU interface and L2 control signals. If this power connects to 3.3V, the relative signals will output 3.3V and accept 3.3V input. If this power connects to 2.5V, the relative signals will output 2.5V and accept 2.5V input.
VCC_B	P	Vcc 3.3V Power for Group B. This power is used for PCI interface and Tag signals. It must connect to 3.3V. The relative signals will output 3.3V and 5V input tolerance.
VCC_C	P	Vcc 3.3V Power for Group C. This power is used for DRAM interface signals during normal operation and suspend refresh. It must connect to 3.3V. The relative signals will output 3.3V and 5V input tolerance.
VDD_5	P	Vcc 5.0V Power for Group A and Group B. This pin supplies the 5V input tolerance circuit and the core power for the internal circuit except the suspend circuit.
VDD_5S	P	Vcc 5.0V Power for Group C. This pin supplies the 5V input tolerance circuit and the core power for the internal suspend circuit.
Vss or Gnd	P	Ground

2.2.1.4 Numerical Pin List

Table 2-4 M1531 Numerical Pin List

No.	Name	Type	No.	Name	Type	No.	Name	Type
A1	--	-	C11	CBEJ3	I/O	F1	BRDYJ	O
A2	PHLDAJ	O	C12	AD28	I/O	F2	BOFFJ	O
A3	AD3	I/O	C13	REQJ1	I	F3	SMIACTJ	I
A4	AD6	I/O	C14	GNTJ0	O	F4	HLOCKJ	I
A5	AD8	I/O	C15	MPD4	I/O	F5	ADSJ	I
A6	AD12	I/O	C16	MD30	I/O	F6	VCC_B	P
A7	PAR	I/O	C17	MD25	I/O	F14	VCC_C	P
A8	TRDYJ	I/O	C18	MD58	I/O	F15	VCC_C	P
A9	AD17	I/O	C19	MD26	I/O	F16	MD50	I/O
A10	AD22	I/O	C20	MD59	I/O	F17	MD18	I/O
A11	AD25	I/O	D1	BEJ6	I	F18	MD51	I/O
A12	AD30	I/O	D2	BEJ5	I	F19	MD19	I/O
A13	REQJ3	I	D3	BEJ4	I	F20	MD52	I/O
A14	GNTJ2	O	D4	AD0	I/O	G1	HD63	I/O
A15	GNTJ3	O	D5	AD1	I/O	G2	CACHEJ	I
A16	MPD2	I/O	D6	AD9	I/O	G3	AHOLD	O
A17	MPD0	I/O	D7	AD14	I/O	G4	KENJ	O
A18	MD61	I/O	D8	LOCKJ	I/O	G5	NAJ	O
A19	MD29	I/O	D9	FRAMEJ	I/O	G6	VCC_A	P
A20	MD62	I/O	D10	AD19	I/O	G15	VCC_C	P

Table 2-4 M1531 Numerical Pin List

No.	Name	Type	No.	Name	Type	No.	Name	Type
B1	BEJ0	I	D11	AD23	I/O	G16	MD15	I/O
B2	PHLDJ	I	D12	AD27	I/O	G17	MD48	I/O
B3	AD2	I/O	D13	REQJ0	I	G18	MD16	I/O
B4	AD5	I/O	D14	MPD7	I/O	G19	MD49	I/O
B5	AD7	I/O	D15	MPD3	I/O	G20	MD17	I/O
B6	AD11	I/O	D16	MD55	I/O	H1	HD60	I/O
B7	CBEJ1	I/O	D17	MD23	I/O	H2	HD61	I/O
B8	DEVSELJ	I/O	D18	MD56	I/O	H3	HD62	I/O
B9	AD16	I/O	D19	MD24	I/O	H4	WRJ	I
B10	AD21	I/O	D20	MD57	I/O	H5	MIOJ	I
B11	AD24	I/O	E1	DCJ	I	H8	GND	P
B12	AD29	I/O	E2	HITMJ	I	H9	GND	P
B13	REQJ2	I	E3	EADSJ	O	H10	GND	P
B14	GNTJ1	O	E4	BEJ7	I	H11	GND	P
B15	MPD5	I/O	E5	RSTJ	I	H12	GND	P
B16	MPD1	I/O	E6	PCIMRQJ	O	H13	GND	P
B17	MD63	I/O	E7	AD13	I/O	H16	MD45	I/O
B18	MD27	I/O	E8	SERRJ	I/O	H17	MD13	I/O
B19	MD60	I/O	E9	IRDYJ	I/O	H18	MD46	I/O
B20	MD28	I/O	E10	AD18	I/O	H19	MD14	I/O
C1	BEJ3	I	E11	PCLKIN	I	H20	MD47	I/O
C2	BEJ2	I	E12	AD26	I/O	J1	HD55	I/O
C3	BEJ1	I	E13	AD31	I/O	J2	HD56	I/O
C4	AD4	I/O	E14	MPD6	I/O	J3	HD57	I/O
C5	CBEJ0	I/O	E15	MD31	I/O	J4	HD58	I/O
C6	AD10	I/O	E16	MD20	I/O	J5	HD59	I/O
C7	AD15	I/O	E17	MD53	I/O	J8	GND	P
C8	STOPJ	I/O	E18	MD21	I/O	J9	GND	P
C9	CBEJ2	I/O	E19	MD54	I/O	J10	GND	P
C10	AD20	I/O	E20	MD22	I/O	J11	GND	P
J12	GND	P	M16	MD35	I/O	T3	HD23	I/O
J13	GND	P	M17	MD3	I/O	T4	HD24	I/O
J16	MD10	I/O	M18	MD36	I/O	T5	HD25	I/O
J17	MD43	I/O	M19	MD4	I/O	T6	HD0	I/O
J18	MD11	I/O	M20	MD37	I/O	T7	A12	I/O
J19	MD44	I/O	N1	HD36	I/O	T8	A5	I/O
J20	MD12	I/O	N2	HD37	I/O	T9	GWEJ	O
K1	HD51	I/O	N3	HD38	I/O	T10	COEJ	O
K2	HD52	I/O	N4	HD39	I/O	T11	CADVJ	O

Table 2-4 M1531 Numerical Pin List

No.	Name	Type	No.	Name	Type	No.	Name	Type
K3	HD53	I/O	N5	HD40	I/O	T12	TWEJ	O
K4	HD54	I/O	N8	GND	P	T13	MAA0	O
K5	HCLKIN	I	N9	GND	P	T14	MAA1	O
K8	GND	P	N10	GND	P	T15	TIO8	I/O
K9	GND	P	N11	GND	P	T16	TIO9	I/O
K10	GND	P	N12	GND	P	T17	TIO10	I/O
K11	GND	P	N13	GND	P	T18	RASJ1	O
K12	GND	P	N15	VDD5S	P	T19	RASJ0	O
K13	GND	P	N16	REQJ4	I/O	T20	CASJ6	O
K16	MD40	I/O	N17	GNTJ4	O	U1	HD16	I/O
K17	MD8	I/O	N18	MD1	I/O	U2	HD17	I/O
K18	MD41	I/O	N19	MD34	I/O	U3	HD18	I/O
K19	MD9	I/O	N20	MD2	I/O	U4	HD19	I/O
K20	MD42	I/O	P1	HD31	I/O	U5	HD20	I/O
L1	HD46	I/O	P2	HD32	I/O	U6	HD1	I/O
L2	HD47	I/O	P3	HD33	I/O	U7	A13	I/O
L3	HD48	I/O	P4	HD34	I/O	U8	A8	I/O
L4	HD49	I/O	P5	HD35	I/O	U9	CCSJ	O
L5	HD50	I/O	P6	VCC_A	P	U10	BWEJ	O
L8	GND	P	P15	VCC_C	P	U11	CADSJ	O
L9	GND	P	P16	32K	I	U12	TIO0	I/O
L10	GND	P	P17	SUSPENDJ	I	U13	TIO1	I/O
L11	GND	P	P18	MD32	I/O	U14	MAB0	O
L12	GND	P	P19	MD0	I/O	U15	MAB1	O
L13	GND	P	P20	MD33	I/O	U16	MA5	O
L16	MD5	I/O	R1	HD26	I/O	U17	MWEJ	I/O
L17	MD38	I/O	R2	HD27	I/O	U18	RASJ4	O
L18	MD6	I/O	R3	HD28	I/O	U19	RASJ3	O
L19	MD39	I/O	R4	HD29	I/O	U20	RASJ2	O
L20	MD7	I/O	R5	HD30	I/O	V1	HD15	I/O
M1	HD41	I/O	R6	VDD5	P	V2	HD14	I/O
M2	HD42	I/O	R7	VCC_A	P	V3	HD13	I/O
M3	HD43	I/O	R14	VCC_B	P	V4	HD6	I/O
M4	HD44	I/O	R15	VCC_C	P	V5	HD3	I/O
M5	HD45	I/O	R16	RASJ6	O	V6	A17	I/O
M8	GND	P	R17	RASJ7	O	V7	A14	I/O
M9	GND	P	R18	CASJ2	O	V8	A10	I/O
M10	GND	P	R19	CASJ7	O	V9	A4	I/O
M11	GND	P	R20	CASJ3	O	V10	A29	I/O

Table 2-4 M1531 Numerical Pin List

No.	Name	Type	No.	Name	Type	No.	Name	Type
M12	GND	P	T1	HD21	I/O	V11	A25	I/O
M13	GND	P	T2	HD22	I/O	V12	A24	I/O
V137	A23	I/O	P16	32K	I	C10	AD20	I/O
V14	TIO2	I/O	Y10	A3	I/O	B10	AD21	I/O
V15	MA2	O	V9	A4	I/O	A10	AD22	I/O
V16	MA4	O	T8	A5	I/O	D11	AD23	I/O
V17	MA8	O	Y9	A6	I/O	B11	AD24	I/O
V18	CASJ5	O	W9	A7	I/O	A11	AD25	I/O
V19	CASJ1	O	U8	A8	I/O	E12	AD26	I/O
V20	RASJ5	O	Y8	A9	I/O	D12	AD27	I/O
W1	HD12	I/O	V8	A10	I/O	C12	AD28	I/O
W2	HD11	I/O	W8	A11	I/O	B12	AD29	I/O
W3	HD10	I/O	T7	A12	I/O	A12	AD30	I/O
W4	HD5	I/O	U7	A13	I/O	E13	AD31	I/O
W5	HD2	I/O	V7	A14	I/O	F5	ADSJ	I
W6	A18	I/O	W7	A15	I/O	G3	AHOLD	O
W7	A15	I/O	Y7	A16	I/O	B1	BEJ0	I
W8	A11	I/O	V6	A17	I/O	C3	BEJ1	I
W9	A7	I/O	W6	A18	I/O	C2	BEJ2	I
W10	A30	I/O	Y6	A19	I/O	C1	BEJ3	I
W11	A31	I/O	Y5	A20	I/O	D3	BEJ4	I
W12	A22	I/O	W13	A21	I/O	D2	BEJ5	I
W13	A21	I/O	W12	A22	I/O	D1	BEJ6	I
W14	TIO4	I/O	V137	A23	I/O	E4	BEJ7	I
W15	TIO6	I/O	V12	A24	I/O	F2	BOFFJ	O
W16	MA3	O	V11	A25	I/O	F1	BRDYJ	O
W17	MA7	O	Y12	A26	I/O	U10	BWEJ	O
W18	MA10	O	Y13	A27	I/O	G2	CACHEJ	I
W19	CASJ0	O	Y11	A28	I/O	U11	CADSJ	O
W20	CASJ4	O	V10	A29	I/O	T11	CADVJ	O
Y1	HD9	I/O	W10	A30	I/O	W19	CASJ0	O
Y2	HD8	I/O	W11	A31	I/O	V19	CASJ1	O
Y3	HD7	I/O	D4	AD0	I/O	R18	CASJ2	O
Y4	HD4	I/O	D5	AD1	I/O	R20	CASJ3	O
Y5	A20	I/O	B3	AD2	I/O	W20	CASJ4	O
Y6	A19	I/O	A3	AD3	I/O	V18	CASJ5	O
Y7	A16	I/O	C4	AD4	I/O	T20	CASJ6	O
Y8	A9	I/O	B4	AD5	I/O	R19	CASJ7	O
Y9	A6	I/O	A4	AD6	I/O	C5	CBEJ0	I/O

Table 2-4 M1531 Numerical Pin List

No.	Name	Type	No.	Name	Type	No.	Name	Type
Y10	A3	I/O	B5	AD7	I/O	B7	CBEJ1	I/O
Y11	A28	I/O	A5	AD8	I/O	C9	CBEJ2	I/O
Y12	A26	I/O	D6	AD9	I/O	C11	CBEJ3	I/O
Y13	A27	I/O	C6	AD10	I/O	U9	CCSJ	O
Y14	TIO3	I/O	B6	AD11	I/O	T10	COEJ	O
Y15	TIO5	I/O	A6	AD12	I/O	E1	DCJ	I
Y16	TIO7	I/O	E7	AD13	I/O	B8	DEVSELJ	I/O
Y17	MA6	O	D7	AD14	I/O	E3	EADSJ	O
Y18	MA9	O	C7	AD15	I/O	D9	FRAMEJ	I/O
Y19	MA11	O	B9	AD16	I/O	H10	GND	P
Y20	--	--	A9	AD17	I/O	H11	GND	P
A1	**--**	--	E10	AD18	I/O	H12	GND	P
Y20	--	--	D10	AD19	I/O	H13	GND	P
H8	GND	P	W2	HD11	I/O	H2	HD61	I/O
H9	GND	P	W1	HD12	I/O	H3	HD62	I/O
J10	GND	P	V3	HD13	I/O	G1	HD63	I/O
J11	GND	P	V2	HD14	I/O	E2	HITMJ	I
J12	GND	P	V1	HD15	I/O	F4	HLOCKJ	I
J13	GND	P	U1	HD16	I/O	E9	IRDYJ	I/O
J8	GND	P	U2	HD17	I/O	G4	KENJ	O
J9	GND	P	U3	HD18	I/O	D8	LOCKJ	I/O
K10	GND	P	U4	HD19	I/O	V15	MA2	O
K11	GND	P	U5	HD20	I/O	W16	MA3	O
K12	GND	P	T1	HD21	I/O	V16	MA4	O
K13	GND	P	T2	HD22	I/O	U16	MA5	O
K8	GND	P	T3	HD23	I/O	Y17	MA6	O
K9	GND	P	T4	HD24	I/O	W17	MA7	O
L10	GND	P	T5	HD25	I/O	V17	MA8	O
L11	GND	P	R1	HD26	I/O	Y18	MA9	O
L12	GND	P	R2	HD27	I/O	W18	MA10	O
L13	GND	P	R3	HD28	I/O	Y19	MA11	O
L8	GND	P	R4	HD29	I/O	T13	MAA0	O
L9	GND	P	R5	HD30	I/O	T14	MAA1	O
M10	GND	P	P1	HD31	I/O	U14	MAB0	O
M11	GND	P	P2	HD32	I/O	U15	MAB1	O
M12	GND	P	P3	HD33	I/O	P19	MD0	I/O
M13	GND	P	P4	HD34	I/O	N18	MD1	I/O
M8	GND	P	P5	HD35	I/O	N20	MD2	I/O
M9	GND	P	N1	HD36	I/O	M17	MD3	I/O

Table 2-4 M1531 Numerical Pin List

No.	Name	Type	No.	Name	Type	No.	Name	Type
N10	GND	P	N2	HD37	I/O	M19	MD4	I/O
N11	GND	P	N3	HD38	I/O	L16	MD5	I/O
N12	GND	P	N4	HD39	I/O	L18	MD6	I/O
N13	GND	P	N5	HD40	I/O	L20	MD7	I/O
N8	GND	P	M1	HD41	I/O	K17	MD8	I/O
N9	GND	P	M2	HD42	I/O	K19	MD9	I/O
C14	GNTJ0	O	M3	HD43	I/O	J16	MD10	I/O
B14	GNTJ1	O	M4	HD44	I/O	J18	MD11	I/O
A14	GNTJ2	O	M5	HD45	I/O	J20	MD12	I/O
A15	GNTJ3	O	L1	HD46	I/O	H17	MD13	I/O
N17	GNTJ4	O	L2	HD47	I/O	H19	MD14	I/O
T9	GWEJ	O	L3	HD48	I/O	G16	MD15	I/O
K5	HCLKIN	I	L4	HD49	I/O	G18	MD16	I/O
T6	HD0	I/O	L5	HD50	I/O	G20	MD17	I/O
U6	HD1	I/O	K1	HD51	I/O	F17	MD18	I/O
W5	HD2	I/O	K2	HD52	I/O	F19	MD19	I/O
V5	HD3	I/O	K3	HD53	I/O	E16	MD20	I/O
Y4	HD4	I/O	K4	HD54	I/O	E18	MD21	I/O
W4	HD5	I/O	J1	HD55	I/O	E20	MD22	I/O
V4	HD6	I/O	J2	HD56	I/O	D17	MD23	I/O
Y3	HD7	I/O	J3	HD57	I/O	D19	MD24	I/O
Y2	HD8	I/O	J4	HD58	I/O	C17	MD25	I/O
Y1	HD9	I/O	J5	HD59	I/O	C19	MD26	I/O
W3	HD10	I/O	H1	HD60	I/O	B18	MD27	I/O
B20	MD28	I/O	B16	MPD1	I/O	W15	TIO6	I/O
A19	MD29	I/O	A16	MPD2	I/O	Y16	TIO7	I/O
C16	MD30	I/O	D15	MPD3	I/O	T15	TIO8	I/O
E15	MD31	I/O	C15	MPD4	I/O	T16	TIO9	I/O
P18	MD32	I/O	B15	MPD5	I/O	T17	TIO10	I/O
P20	MD33	I/O	E14	MPD6	I/O	A8	TRDYJ	I/O
N19	MD34	I/O	D14	MPD7	I/O	T12	TWEJ	O
M16	MD35	I/O	U17	MWEJ	I/O	F14	VCC_C	P
M18	MD36	I/O	G5	NAJ	O	F15	VCC_C	P
M20	MD37	I/O	A7	PAR	I/O	F6	VCC_B	P
L17	MD38	I/O	E6	PCIMRQJ	O	G15	VCC_C	P
L19	MD39	I/O	E11	PCLKIN	I	G6	VCC_A	P
K16	MD40	I/O	A2	PHLDAJ	O	P6	VCC_A	P
K18	MD41	I/O	B2	PHLDJ	I	P15	VCC_C	P
K20	MD42	I/O	T19	RASJ0	O	R14	VCC_B	P

Table 2-4 M1531 Numerical Pin List

No.	Name	Type	No.	Name	Type	No.	Name	Type
J17	MD43	I/O	T18	RASJ1	O	R15	VCC_C	P
J19	MD44	I/O	U20	RASJ2	O	R7	VCC_A	P
H16	MD45	I/O	U19	RASJ3	O	R6	VDD5	P
H18	MD46	I/O	U18	RASJ4	O	N15	VDD5S	P
H20	MD47	I/O	V20	RASJ5	O	H4	WRJ	I
G17	MD48	I/O	R16	RASJ6	O	--	--	--
G19	MD49	I/O	R17	RASJ7	O	--	--	--
F16	MD50	I/O	D13	REQJ0	I	--	--	--
F18	MD51	I/O	C13	REQJ1	I	--	--	--
F20	MD52	I/O	B13	REQJ2	I	--	--	--
E17	MD53	I/O	A13	REQJ3	I	--	--	--
E19	MD54	I/O	N16	REQJ4	I/O	--	--	--
D16	MD55	I/O	E5	RSTJ	I	--	--	--
D18	MD56	I/O	E8	SERRJ	I/O	--	--	--
D20	MD57	I/O	F3	SMIACTJ	I	--	--	--
C18	MD58	I/O	C8	STOPJ	I/O	--	--	--
C20	MD59	I/O	P17	SUSPENDJ	I	--	--	--
B19	MD60	I/O	U12	TIO0	I/O	--	--	--
A18	MD61	I/O	U13	TIO1	I/O	--	--	--
A20	MD62	I/O	V14	TIO2	I/O	--	--	--
B17	MD63	I/O	Y14	TIO3	I/O	--	--	--
H5	MIOJ	I	W14	TIO4	I/O	--	--	--
A17	MPD0	I/O	Y15	TIO5	I/O	--	--	--

2.2.2 M1533

The M1533 is a bridge between PCI and ISA bus, providing full PCI and ISA compatible functions. This chip has Integrated System Peripherals (ISP) (2 x 82C59 and serial interrupt, 1 x 82C54), advanced features (Type F and Distributed DMA) in the DMA controller (2 x 82C54), PS/2 keyboard/mouse controller, two-channel dedicated IDE master controller with Ultra-33 specification, System Management Bus (SMB), and two OpenHCI 1.0a USB ports. The ACPI (Advanced Configuration and Power Interface) and PCI 2.1 (Delayed Transaction & Passive Release) specification have also been implemented. Furthermore, this chip supports the Advanced Programmable Interrupt Controller (APIC) interface for Multiple-Processors system.

The M1533 also supports the deep flexible green function for the best green system. It can connect to the ALi Pentium North Bridge (M1521/M1531/M1541) and ALi Pentium Pro North Bridge (M1615) to provide the best system solution. One eight-byte bidirectional line buffer is provided for ISA/DMA master memory read/writes; one 32-bit wide posted write buffer is provided for PCI memory write & I/O write (for audio) cycles to the ISA bus, to provide a PCI to ISA IRQ routing table, and
level-to-edge trigger transfer.

The chip provides two extra IRQ lines and one programmable chip select for motherboard Plug-and-Play functions. The interrupt lines can be routed to any of the available ISA interrupts. The on-chip IDE controller supports two separate IDE connectors for up to four IDE devices providing an interface for IDE hard disks and CD ROMs. The Ultra 33 specification (that supports the 33 MB/second transfer rate) has been implemented at this IDE controller. The ATA bus pins and the buffer (read ahead and posted write) are all dedicated for separate channel to improve the performance of IDE master.

The M1533 supports Super Green function for Intel and Intel compatible CPUs. It implements SMI or SCI (System Controller Interrupt) to meet the ACPI specification. It also meets the requirement for OnNow design initiative. It also features powerful power management for power saving including On, Standby, Sleeping, SoftOff, and Mechanical Off states. To control the CPU power consumption, it provides CPU clock control (STPCLKJ). The STPCLKJ can be active (low) or inactive (high) in turn by throttling control. In addition, the M1533 offers the most flexible system clock design. It can be programmed to stop the CPU Clock, PCI Clock, the Clock cell, or to reduce the Clock frequency. The PBSRAM (Pipelined-burst SRAM) doze mode is also supported.

The M1533 is includes a PS/2 keyboard/mouse controller, SMBus, two OpenHCI 1.0a USB ports, and the dedicated GPIO (General Purpose Input/Output) pins. These components enable the chip to implement the best green and cost/performance system.

2.2.2.1 Features

- Provides a bridge between the PCI bus and ISA bus for both Pentium and Pentium Pro systems
- PCI interface
  - PCI master and slave interface
  - PCI master and slave initiated termination
  - PCI spec. 2.1 compliant (Delayed Transaction support)
- Buffers control
  - 8-byte bidirectional line buffers for DMA/ISA memory read/write cycles to PCI bus
  - 32-bit posted write buffer for PCI memory write and I/O data write (for sound card) to ISA bus
- Provides steerable PCI interrupts for PCI device plug-and-play
  - Up to eight PCI interrupt routing
  - Level-to-edge trigger transfer
- Enhanced DMA controller
  - Provides 7 programmable channels: 4 for 8-bit data size, 3 for 16-bit data size
  - 32-bit addressability
  - Provides compatible DMA transfers
  - Provides Type F transfers
- Interrupt controller
  - Provides 14 interrupt channels

- Independent programmable level/edge triggered channels

- Counter/Timers
  - 8254 compatible timers for System Timer, Refresh Request, Speaker Output Use
- Distributed DMA supported
  - 7 DMA Channels can be arbitrarily programmed as distributed channel
- Serialized IRQ supported
  - Quiet/Continuous mode
  - Programmable (default 21) IRQ/DATA frames
  - Programmable START frame pulse width
- Plug-and-Play port supported
  - One programmable chip select
  - Two steerable interrupt request lines
- Built-in keyboard controller
  - Built-in PS/2/AT keyboard and PS/2 mouse controller
- Supports up to 256-KB ROM size decoding
- Supports positive/subtractive decode for ISA device
- PMU features
  - Full-support for ACPI and OS directed power management
  - CPU SMM Legacy mode and SMI feature supported
  - Supports programmable STPCLKJ: throttle/CKONSTP/CKOFFSTP control
  - Supports I/O trap for I/O restart feature
  - PMU operation states :
    - On
    - Standby
    - Sleeping (Power-On Suspend)
    - Suspend (Suspend to DRAM)
    - Suspend to HDD
    - Soft Off
    - Mechanical Off
  - APM state detection and control logic supported
  - Global and local device power control logic
  - Ten Programmable Timers: Standby / LB / LLB / APMA / APMB / Global_Display / Primary_IDE / Secondary_IDE / SIO&Audio / Programmable IO Region
  - Provides system activity and display activity monitorings, including:
    - Video
    - Audio

  - Hard disk
  - Floppy
  - Serial ports
  - Parallel port
  - Keyboard
  - Six programmable I/O groups
  - Three programmable memory spaces
- Provides hot plugging events detection
  - CRT connector
  - AC power
  - Docking insert
  - Eject
  - Setup button
  - Hot key press
- Multiple external wakeup events of Standby mode
  - Power button
  - Cover open
  - Modem ring
  - RTC alarm
  - EXTSW
  - DRQ2
- Suspend wakeup detected
  - Hot key
  - Modem ring
  - RTC alarm
  - Cover open
  - Docking insert
  - Power button
  - USB events
  - IRQ
  - EJECT
  - ACPWR
  - GPIO[19:16] event
    - Two-level battery warning monitor
- Thermal alarm supported
- Clock generator control logic supported
  - CPUCLK stop control
  - PCICLK stop control
  - PLL stop control
  - Down frequency control

- L2 cache power down and PCI CLKRUN control logic supported
- 21 general purpose input signals, 24 general purpose output signals, 20 general purpose input/output signals
- 16 external expandable general purpose inputs, 16 external expandable general purpose outputs
- LCD control
- All registers readable/restorable for proper resume from Suspend state

- Built-in PCI IDE controller
  - Supports Ultra 33 Synchronous DMA Mode transfers up to Mode 2 Timing (33 MB/sec)
  - Supports PIO Modes up to Mode 5 timings, and Multiword DMA Mode 0, 1 ,2 with independent timing of up to 4 drives
  - Integrated 10 x 32-bit read ahead & posted write buffers for each channel (total: 20 Dwords)
  - Dedicated pins of ATA interface for each channel
  - Supports tri-state IDE signals for swap bay
- USB interface
  - One root hub with two USB ports based on OpenHCI 1.0a specification
  - Supports FS (12Mbits/sec) and LS (1.5Mbits/sec) serial transfer
  - Supports Legacy keyboard and mouse software with USB-based keyboard and mouse
- SMBus interface
  - System Management Bus interface which meets the v1.0 specification
- External APIC interface supported
- 328-pin (27mm x 27mm) BGA package

2.2.2.2 Pin Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	NC	AD21	AD18	CBEJ2	STOPJ	AD14	AD9	AD5	AD0	SIDED7	SIDED10	SIDED2	SIDED15	SIDEAKJ	SIDECS3J	PIDED6	PIDED10	PIDED3	NC	NC
B	NC	AD22	AD19	AD16	**DEVSELJ**	AD15	AD10	AD6	AD1	PHLDJ	SIDED5	SIDED12	SIDED0	**SIDEIRDY**	SIDECS1J	**PIDED9**	PIDED11	PIDED13	PIDED2	PIDED14
C	CBEJ3	AD23	AD20	AD17	TRDYJ	CBEJ1	AD11	AD7	AD2	PHLDAJ	SIDED9	SIDED3	SIDED14	SIDEIORJ	SIDEA2	PIDED5	PIDED4	PIDED1	PIDED15	PIDED0
D	AD26	AD25	AD24	PCIRSTJ	IRDYJ	PAR	AD12	CBEJ0	AD3	CLKRUNJ	SIDED6	SIDED11	SIDED1	**SIDEIOWJ**	SIDEA0	PIDED8	PIDED12	PIDEA1	PIDEA0	PIDEA2
E	AD29	AD28	AD27	AD30	FRAMEJ	SERRJ	AD13	AD8	AD4	PCICLK	SIDED8	SIDED4	SIDED13	**SIDEDRQ**	SIDEA1	PIDED7	PIDEAKJ	PIDECS1J	PIDECS3J	INTR
F	USBCLK	GPO8	AD31	INTAJ	INTBJ	VCC_B									VCC_D	VCC_E	PIDEIOWJ	PIDEIRDY	NMI	SMIJ	IGNNEJ
G	USBP0-	USBP0+	GPO4	INTCJ	INTDJ	VCC_B				**M1533**					VCC_3C	PIDEDRQ	PIDEIORJ	CPURST	A20MJ	INIT
H	USBP1-	USBP1+	GPI3	GPO3	GPO2			GND	GND	GND	GND	GND	GND			IRQ13	STPCLK	SMBDATA	SMBCLK	RI
J	SD7	RSTDRV	IOCHKJ	GPI1	GPI0			GND	GND	GND	GND	GND	GND			GPO1	GPO20	**GPIO19**	GPIO18	GPIO17
K	SD5	IRQ9	SD6	MSCLK	MSDATA			GND	GND	GND	GND	GND	GND			LLBJ	DOCKJ	GPIO16	GPIO15	GPIO14
L	SD3	DREQ2	SD4	KBCLK	KBDATA			GND	GND	GND	GND	GND	GND			IRQ8J	SUSTAT1J	PWRBTNJ	GPIO13	GPIO12
M	IOCHRDY	SD0	SD1	NOWSJ	SD2			GND	GND	GND	GND	GND	GND			PWG	HOTKEYJ	**RSMRSTJ**	LBJ	LID
N	IOWJ	SA19	**SMEMRJ**	AEN	SMEMWJ			GND	GND	GND	GND	GND	GND		VDD5S	SIRQI	SIRQII	OSC32KII	OSC32KI	OSC32KO
P	SA16	DACKJ3	SA17	IORJ	SA18	VCC_A									VCC_C	GPO19	GPO18	GPO23	GPO22	GPO21
R	DREQ1	SA14	**DACKJ1**	SA15	DREQ3	VDD5	VCC_A							**Vcc_3A**	VCC_A	GPO17	GPO16	GPO15	GPO14	GPO13
T	REFSHJ	SA13	IRQ6	IRQ4	**DACKJ2**	BALE	LA23	LA20	DACKJ0	MEMWJ	DREQ6	ROMKBCSJ	RTCAS	**RTCRW**	IRQ1I	GPO12	GPO11	GPO10	GPO9	GPO7
U	SA12	IRQ7	IRQ5	IRQ3	TC	OSC14M	IRQ10	IRQ15	LA17	**DREQ5**	SD10	SD12	RTCDS	XD0	XD4	EJECT	GPIO11	GPO6	GPO5	GPO0
V	SYSCLK	SA10	SA8	SA5	SA2	M16J	LA22	LA19	DREQ0	SD8	DACKJ7	SD13	SPKR	XD1	XD5	ACPWR	GPI6	GPIO8	GPIO9	GPI010
W	SA11	SA9	SA7	SA4	SA1	SBHEJ	IRQ11	IRQ14	MEMRJ	**DACKJ6**	SD11	SD14	SPLED	XD2	XD6	SETUPJ	GPI4	GPI7	GPI8	NC
Y	NC	NC	SA6	SA3	SA0	IO16J	LA21	LA18	DACKJ5	SD9	DREQ7	SD15	EXTSW	XD3	XD7	THRMJ	CRT	GPI2	GPI5	NC

Figure 2-3 M1533 Pin Diagram (Top View)

2.2.2.3 Numerical Pin List

Table 2-5 M1533 Numerical Pin List

No.	Name	Type	No.	Name	Type	No.	Name	Type
A1	**--**	--	C11	SIDED9	I/O	F1	USBCLK	I
A2	AD21	I/O	C12	SIDED3	I/O	F2	GPO8	O
A3	AD18	I/O	C13	SIDED14	I/O	F3	AD31	I/O
A4	CBEJ2	I/O	C14	SIDEIORJ	O	F4	INTAJ	I
A5	STOPJ	I/O	C15	SIDEA2	O	F5	INTBJ	I/O
A6	AD14	I/O	C16	PIDED5	I/O	F6	VCC	P
A7	AD9	I/O	C17	PIDED4	I/O	F14	VCC	P
A8	AD5	I/O	C18	PIDED1	I/O	F15	VCC	P
A9	AD0	I/O	C19	PIDED15	I/O	F16	PIDEIOWJ	O
A10	SIDED7	I/O	C20	PIDED0	I/O	F17	PIDERDY	I
A11	SIDED10	I/O	D1	AD26	I/O	F18	NMI	O
A12	SIDED2	I/O	D2	AD25	I/O	F19	SMIJ	O
A13	SIDED15	I/O	D3	AD24	I/O	F20	IGNNEJ	O
A14	SIDEAKJ	O	D4	PCIRSTJ	O	G1	USBP0-	I/O
A15	SIDECS3J	O	D5	IRDYJ	I/O	G2	USBP0+	I/O
A16	PIDED6	I/O	D6	PAR	I/O	G3	GPO4	O
A17	PIDED10	I/O	D7	AD12	I/O	G4	INTCJ	I/O
A18	PIDED3	I/O	D8	CBEJ0	I/O	G5	INTDJ	I/O
A19	--	-	D9	AD3	I/O	G6	VCC	P
A20	--	-	D10	CLKRUNJ	I/O	G15	VCC	P
B1	**--**	-	D11	SIDED6	I/O	G16	PIDEDRQ	I
B2	AD22	I/O	D12	SIDED11	I/O	G17	PIDEIORJ	O
B3	AD19	I/O	D13	SIDED1	I/O	G18	CPURST	O
B4	AD16	I/O	D14	SIDEIOWJ	O	G19	A20MJ	O
B5	DEVSELJ	I/O	D15	SIDEA0	O	G20	INIT	O
B6	AD15	I/O	D16	PIDED8	I/O	H1	USBP1-	I/O
B7	AD10	I/O	D17	PIDED12	I/O	H2	USBP1+	I/O
B8	AD6	I/O	D18	PIDEA1	O	H3	GPI3	I
B9	AD1	I/O	D19	PIDEA0	O	H4	GPO3	O
B10	PHOLDJ	O	D20	PIDEA2	O	H5	GPO2	O
B11	SIDED5	I/O	E1	AD29	I/O	H8	GND	P
B12	SIDED12	I/O	E2	AD28	I/O	H9	GND	P
B13	SIDED0	I/O	E3	AD27	I/O	H10	GND	P
B14	SIDERDY	I	E4	AD30	I/O	H11	GND	P
B15	SIDECS1J	O	E5	FRAMEJ	I/O	H12	GND	P
B16	PIDED9	I/O	E6	SERRJ	I	H13	GND	P
B17	PIDED11	I/O	E7	AD13	I/O	H16	IRQ13	I/O
B18	PIDED13	I/O	E8	AD8	I/O	H17	STPCLK	O

Table 2-5 M1533 Numerical Pin List

No.	Name	Type	No.	Name	Type	No.	Name	Type
B19	PIDED2	I/O	E9	AD4	I/O	H18	SMBDATA	I/O
B20	PIDED14	I/O	E10	PCICLK	I	H19	SMBCLK	I/O
C1	CBEJ3	I/O	E11	SIDED8	I/O	H20	RI	I
C2	AD23	I/O	E12	SIDED4	I/O	J1	SD7	I/O
C3	AD20	I/O	E13	SIDED13	I/O	J2	RSTDRV	O
C4	AD17	I/O	E14	SIDEDRQ	I	J3	IOCHKJ	I/O
C5	TRDYJ	I/O	E15	SIDEA1	O	J4	GPI1	I
C6	CBEJ1	I/O	E16	PIDED7	I/O	J5	GPI0	I
C7	AD11	I/O	E17	PIDEAKJ	O	J8	GND	P
C8	AD7	I/O	E18	PIDECS1J	O	J9	GND	P
C9	AD2	I/O	E19	PIDECS3J	O	J10	GND	P
C10	PHLDAJ	I	E20	INTR	O	J11	GND	P
J12	GND	P	M16	PWG	I	T3	IRQ6	I/O
J13	GND	P	M17	HOTKEYJ	I	T4	IRQ4	I/O
J16	GPO1	O	M18	RSMRSTJ	I	T5	DACKJ2	O
J17	GPO20	O	M19	LBJ	I	T6	BALE	O
J18	GPIO19	I/O	M20	LID	I	T7	LA23	I/O
J19	GPIO18	I/O	N1	IOWJ	I/O	T8	LA20	I/O
J20	GPIO17	I/O	N2	SA19	O	T9	DACKJ0	O
K1	SD5	I/O	N3	SMEMRJ	O	T10	MEMWJ	I/O
K2	IRQ9	I/O	N4	AEN	O	T11	DREQ6	I
K3	SD6	I/O	N5	SMEMWJ	O	T12	ROMKBCSJ	O
K4	MSCLK	O	N8	GND	P	T13	RTCAS	O
K5	MSDATA	I/O	N9	GND	P	T14	RTCRW	O
K8	GND	P	N10	GND	P	T15	IRQ1I	I/O
K9	GND	P	N11	GND	P	T16	GPO12	O
K10	GND	P	N12	GND	P	T17	GPO11	O
K11	GND	P	N13	GND	P	T18	GPO10	O
K12	GND	P	N15	VDD5S	P	T19	GPO9	O
K13	GND	P	N16	SIRQI	I	T20	GPO7	O
K16	LLBJ	I	N17	SIRQII	I	U1	SA12	I/O
K17	DOCKJ	I	N18	OSC32KII	I	U2	IRQ7	I/O
K18	GPIO16	I/O	N19	OSC32KI	I	U3	IRQ5	I/O
K19	GPIO15	I/O	N20	OSC32KO	O	U4	IRQ3	I/O
K20	GPIO14	I/O	P1	SA16	I/O	U5	TC	O
L1	SD3	I/O	P2	DACKJ3	O	U6	OSC14M	I
L2	DREQ2	I	P3	SA17	O	U7	IRQ10	I/O
L3	SD4	I/O	P4	IORJ	I/O	U8	IRQ15	I/O
L4	KBCLK	I/O	P5	SA18	O	U9	LA17	I/O

Table 2-5 M1533 Numerical Pin List

No.	Name	Type	No.	Name	Type	No.	Name	Type
L5	KBDATA	I/O	P6	VCC	P	U10	DREQ5	I
L8	GND	P	P15	VCC	P	U11	SD10	I/O
L9	GND	P	P16	GPO19	O	U12	SD12	I/O
L10	GND	P	P17	GPO18	O	U13	RTCDS	O
L11	GND	P	P18	GPO23	O	U14	XD0	I/O
L12	GND	P	P19	GPO22	O	U15	XD4	I/O
L13	GND	P	P20	GPO21	O	U16	EJECT	I
L16	IRQ8J	I	R1	DREQ1	I	U17	GPIO11	I/O
L17	SUSTAT1J	O	R2	SA14	I/O	U18	GPO6	O
L18	PWRBTNJ	I	R3	DACKJ1	O	U19	GPO5	O
L19	GPIO13	I/O	R4	SA15	I/O	U20	GPO0	O
L20	GPIO12	I/O	R5	DREQ3	I	V1	SYSCLK	O
M1	IOCHRDY	I/O	R6	VDD5	P	V2	SA10	I/O
M2	SD0	I/O	R7	VCC	P	V3	SA8	I/O
M3	SD1	I/O	R14	VCC	P	V4	SA5	I/O
M4	NOWSJ	I	R15	VCC	P	V5	SA2	I/O
M5	SD2	I/O	R16	GPO17	O	V6	M16J	I/O
M8	GND	P	R17	GPO16	O	V7	LA22	I/O
M9	GND	P	R18	GPO15	O	V8	LA19	I/O
M10	GND	P	R19	GPO14	O	V9	DREQ0	I
M11	GND	P	R20	GPO13	O	V10	SD8	I/O
M12	GND	P	T1	REFSHJ	I/O	V11	DACKJ7	O
M13	GND	P	T2	SA13	I/O	V12	SD13	I/O
V13	SPKR	O	A20	--	-	R3	DACKJ1	O
V14	XD1	I/O	B1	**--**	-	T5	DACKJ2	O
V15	XD5	I/O	W20	--	-	P2	DACKJ3	O
V16	ACPWR	I	Y1	**--**	-	Y9	DACKJ5	O
V17	GPI6	I	Y2	--	-	W10	DACKJ6	O
V18	GPIO8	I/O	Y20	--	-	V11	DACKJ7	O
V19	GPIO9	I/O	G19	A20MJ	O	B5	DEVSELJ	I/O
V20	GPIO10	I/O	V16	ACPWR	I	K17	DOCKJ	I
W1	SA11	I/O	A9	AD0	I/O	V9	DREQ0	I
W2	SA9	I/O	B9	AD1	I/O	R1	DREQ1	I
W3	SA7	I/O	C9	AD2	I/O	L2	DREQ2	I
W4	SA4	I/O	D9	AD3	I/O	R5	DREQ3	I
W5	SA1	I/O	E9	AD4	I/O	U10	DREQ5	I
W6	SBHEJ	I/O	A8	AD5	I/O	T11	DREQ6	I
W7	IRQ11	I/O	B8	AD6	I/O	Y11	DREQ7	I
W8	IRQ14	I/O	C8	AD7	I/O	U16	EJECT	I

Table 2-5 M1533 Numerical Pin List

No.	Name	Type	No.	Name	Type	No.	Name	Type
W9	MEMRJ	I/O	E8	AD8	I/O	Y13	EXTSW	I
W10	DACKJ6	O	A7	AD9	I/O	E5	FRAMEJ	I/O
W11	SD11	I/O	B7	AD10	I/O	H10	GND	P
W12	SD14	I/O	C7	AD11	I/O	H11	GND	P
W13	SPLED	O	D7	AD12	I/O	H12	GND	P
W14	XD2	I/O	E7	AD13	I/O	H13	GND	P
W15	XD6	I/O	A6	AD14	I/O	H8	GND	P
W16	SETUPJ	I	B6	AD15	I/O	H9	GND	P
W17	GPI4	I	B4	AD16	I/O	J10	GND	P
W18	GPI7	I	C4	AD17	I/O	J11	GND	P
W19	GPI8	I	A3	AD18	I/O	J12	GND	P
W20	--	-	B3	AD19	I/O	J13	GND	P
Y1	**--**	-	C3	AD20	I/O	J8	GND	P
Y2	--	-	A2	AD21	I/O	J9	GND	P
Y3	SA6	I/O	B2	AD22	I/O	K10	GND	P
Y4	SA3	I/O	C2	AD23	I/O	K11	GND	P
Y5	SA0	I/O	D3	AD24	I/O	K12	GND	P
Y6	IO16J	I	D2	AD25	I/O	K13	GND	P
Y7	LA21	I/O	D1	AD26	I/O	K8	GND	P
Y8	LA18	I/O	E3	AD27	I/O	K9	GND	P
Y9	DACKJ5	O	E2	AD28	I/O	L10	GND	P
Y10	SD9	I/O	E1	AD29	I/O	L11	GND	P
Y11	DREQ7	I	E4	AD30	I/O	L12	GND	P
Y12	SD15	I/O	F3	AD31	I/O	L13	GND	P
Y13	EXTSW	I	N4	AEN	O	L8	GND	P
Y14	XD3	I/O	T6	BALE	O	L9	GND	P
Y15	XD7	I/O	D8	CBEJ0	I/O	M10	GND	P
Y16	THRMJ	I	C6	CBEJ1	I/O	M11	GND	P
Y17	CRT	I	A4	CBEJ2	I/O	M12	GND	P
Y18	GPI2	I	C1	CBEJ3	I/O	M13	GND	P
Y19	GPI5	I	D10	CLKRUNJ	I/O	M8	GND	P
Y20	--	-	G18	CPURST	O	M9	GND	P
A1	**--**	-	Y17	CRT	I	N10	GND	P
A19	--	-	T9	DACKJ0	O	N11	GND	P

Table 2-5 M1533 Numerical Pin List

No.	Name	Type	No.	Name	Type
N12	GND	P	J17	GPO20/SLEEPJ	O
N13	GND	P	P20	GPO21/OFF_PWR0	O
N8	GND	P	P19	GPO22/OFF_PWR1	O
N9	GND	P	P18	GPO23/OFF_PWR2	O
J5	GPI0/OVCRJ0	I	M17	HOTKEYJ	I
J4	GPI1/OVCRJ1	I	F20	IGNNEJ	O
Y18	GPI2/SERIRQ	I	G20	INIT	O
H3	GPI3/PCIREQJ	I	F4	INTAJ	I
W17	GPI4/POSSTA	I	F5	INTBJ	I/O
Y19	GPI5/VCSJ	I	G4	INTCJ	I/O
V17	GPI6/FPVEE	I	G5	INTDJ	I/O
W18	GPI7/SMBEVENTJ	I	E20	INTR	O
W19	GPI8	I	Y6	IO16J	I
V18	GPIO8	I/O	M1	IOCHRDY	I/O
V19	GPIO9	I/O	J3	IOCHKJ	I/O
V20	GPIO10	I/O	P4	IORJ	I/O
U17	GPIO11	I/O	N1	IOWJ	I/O
L20	GPIO12/BATSEL0	I/O	D5	IRDYJ	I/O
L19	GPIO13/BATSEL1	I/O	T15	IRQ1I/KBINH	I/O
K20	GPIO14/BATSEL2	I/O	U4	IRQ3	I/O
K19	GPIO15/BATSEL3	I/O	T4	IRQ4	I/O
K18	GPIO16	I/O	U3	IRQ5	I/O
J20	GPIO17	I/O	T3	IRQ6	I/O
J19	GPIO18	I/O	U2	IRQ7	I/O
J18	GPIO19	I/O	L16	IRQ8J	I
U20	GPO0/PCSJ	O	K2	IRQ9	I/O
J16	GPO1/ZZ	O	U7	IRQ10	I/O
H5	GPO2/CPU_STPJ	O	W7	IRQ11	I/O
H4	GPO3/PCI_STPJ	O	H16	IRQ13/FERRJ	I/O
G3	GPO4/SLOWDWN	O	W8	IRQ14	I/O
U19	GPO5/CCFT	O	U8	IRQ15	I/O
U18	GPO6/DISPLAY	O	L4	KBCLK/GPI9	I/O
T20	GPO7/CONTRAST	O	L5	KBDATA/GPI10	I/O
F2	GPO8/AMSTATJ	O	U9	LA17	I/O
T19	GPO9/SQWO	O	Y8	LA18	I/O
T18	GPO10/GPIORBJ	O	V8	LA19	I/O
T17	GPO11/GPIOWB	O	T8	LA20	I/O
T16	GPO12/XDIR	O	Y7	LA21	I/O

Table 2-5 M1533 Numerical Pin List

No.	Name	Type	No.	Name	Type
R20	GPO13/IRQ1O	O	V7	LA22	I/O
R19	GPO14/IRQ12O	O	T7	LA23	I/O
R18	GPO15/IRQ0	O	M19	LBJ	I
R17	GPO16APICCSJ	O	M20	LID	I
R16	GPO17/APICGNTJ	O	K16	LLBJ	I
P17	GPO18/BIOSA16	O	V6	M16J	I/O
P16	GPO19/BIOSA17	O	W9	MEMRJ	I/O

Table 2-5 M1533 Numerical Pin List

No.	Name	Type	No.	Name	Type	No.	Name	Type
T10	MEMWJ	I/O	V5	SA2	I/O	A11	SIDED10	I/O
K4	MSCLK/GPI11	O	Y4	SA3	I/O	D12	SIDED11	I/O
K5	MSDATA/IRQ12I	I/O	W4	SA4	I/O	B12	SIDED12	I/O
F18	NMI	O	V4	SA5	I/O	E13	SIDED13	I/O
M4	NOWSJ	I	Y3	SA6	I/O	C13	SIDED14	I/O
U6	OSC14M	I	W3	SA7	I/O	A13	SIDED15	I/O
N19	OSC32KI	I	V3	SA8	I/O	A14	SIDEAKJ	O
N18	OSC32KII	I	W2	SA9	I/O	E14	SIDEDRQ	I
N20	OSC32KO	O	V2	SA10	I/O	B14	SIDERDY	I
D6	PAR	I/O	W1	SA11	I/O	C14	SIDEIORJ	O
E10	PCICLK	I	U1	SA12	I/O	D14	SIDEIOWJ	O
D4	PCIRSTJ	O	T2	SA13	I/O	N16	SIRQI	I
C10	PHLDAJ	I	R2	SA14	I/O	N17	SIRQII	I
B10	PHOLDJ	O	R4	SA15	I/O	H19	SMBCLK	I/O
D19	PIDEA0	O	P1	SA16	I/O	H18	SMBDATA	I/O
D18	PIDEA1	O	P3	SA17	O	N3	SMEMRJ	O
D20	PIDEA2	O	P5	SA18	O	N5	SMEMWJ	O
E18	PIDECS1J	O	N2	SA19	O	F19	SMIJ	O
E19	PIDECS3J	O	W6	SBHEJ	I/O	V13	SPKR	O
C20	PIDED0	I/O	M2	SD0/GPIO0	I/O	W13	SPLED	O
C18	PIDED1	I/O	M3	SD1/GPIO1	I/O	A5	STOPJ	I/O
B19	PIDED2	I/O	M5	SD2/GPIO2	I/O	H17	STPCLKJ	O
A18	PIDED3	I/O	L1	SD3/GPIO3	I/O	L17	SUSTAT1J	O
C17	PIDED4	I/O	L3	SD4/GPIO4	I/O	V1	SYSCLK	O
C16	PIDED5	I/O	K1	SD5/GPIO5	I/O	U5	TC	O
A16	PIDED6	I/O	K3	SD6/GPIO6	I/O	Y16	THRMJ	I
E16	PIDED7	I/O	J1	SD7/GPIO7	I/O	C5	TRDYJ	I/O

Table 2-5 M1533 Numerical Pin List

No.	Name	Type	No.	Name	Type	No.	Name	Type
D16	PIDED8	I/O	V10	SD8	I/O	F1	USBCLK	I
B16	PIDED9	I/O	Y10	SD9	I/O	G2	USBP0+	I/O
A17	PIDED10	I/O	U11	SD10	I/O	G1	USBP0-	I/O
B17	PIDED11	I/O	W11	SD11	I/O	H2	USBP1+	I/O
D17	PIDED12	I/O	U12	SD12	I/O	H1	USBP1-	I/O
B18	PIDED13	I/O	V12	SD13	I/O	F14	VCC	P
B20	PIDED14	I/O	W12	SD14	I/O	F15	VCC	P
C19	PIDED15	I/O	Y12	SD15	I/O	F6	VCC	P
E17	PIDEAKJ	O	E6	SERRJ	I	G15	VCC	P
G16	PIDEDRQ	I	W16	SETUPJ	I	G6	VCC	P
G17	PIDEIORJ	O	D15	SIDEA0	O	P6	VCC	P
F16	PIDEIOWJ	O	E15	SIDEA1	O	P15	VCC	P
F17	PIDERDY	I	C15	SIDEA2	O	R14	VCC	P
M16	PWG	I	B15	SIDECS1J	O	R15	VCC	P
L18	PWRBTNJ	I	A15	SIDECS3J	O	R7	VCC	P
T1	REFSHJ	I/O	B13	SIDED0	I/O	R6	VDD5	P
H20	RI	I	D13	SIDED1	I/O	N15	VDD5S	P
T12	ROMKBCSJ	O	A12	SIDED2	I/O	U14	XD0	I/O
M18	RSMRSTJ	I	C12	SIDED3	I/O	V14	XD1	I/O
J2	RSTDRV	O	E12	SIDED4	I/O	W14	XD2	I/O
T13	RTCAS	O	B11	SIDED5	I/O	Y14	XD3	I/O
U13	RTCDS	O	D11	SIDED6	I/O	U15	XD4	I/O
T14	RTCRW	O	A10	SIDED7	I/O	V15	XD5	I/O
Y5	SA0	I/O	E11	SIDED8	I/O	W15	XD6	I/O
W5	SA1	I/O	C11	SIDED9	I/O	Y15	XD7	I/O

2.3 FDC37C672

The FDC37C672 is a 100-pin enhanced super I/O controller with Fast IR.

2.3.1 Features

- 5 Volt Operation
- PC97 Compliant
- ISA Plug and Play Compatible Register Set
- Intelligent Auto Power Management
- Shadowed Write-only Registers for ACPI Compliance
- System Management Interrupt, Watchdog Timer
- 2.88MB Super I/O Floppy Disk Controller
  - Licensed CMOS 765B Floppy Disk Controller
  - Software and Register Compatible with SMC's Proprietary 82077AA Compatible Core
  - Supports Two Floppy Drives Directly
  - Configurable Open Drain/Push-pull Output Drivers
  - Supports Vertical Recording Format
  - 16yte Data FIFO
  - 100% IBM2 Compatibility
  - Detects All Overrun and Underrun Conditions
  - Sophisticated Power Control Circuitry {PCC} Including Multiple Power-down Modes for Reduced Power Consumption
  - DMA Enable Logic
  - Data Rate and Drive Control Registers
  - 480 Address, Up to Eight IRQ and Three DMA Options
- Floppy Disk Available on Parallel Port Pins
- Enhanced Digital Data Separator
  - 2 Mbps, 1 Mbps, 500 Kbps, 300 Kbps, 250 Kbps Data Rates
  - Programmable Precompensation Modes
- Keyboard Controller
  - 8042 Software Compatible
  - 8it Microcomputer
  - 2k Bytes of Program ROM
  - 256 Bytes of Data RAM

- Four Open Drain Outputs Dedicated for Keyboard/Mouse Interface
- Asynchronous Access to Two Data Registers and One Status Register
- Supports Interrupt and Polling Access
- 8it Counter Timer
- Port 92 Support
- 8042 P12 and P16 Outputs

- Serial Ports
  - Two Full Function Serial Ports
  - High Speed NS16C550 Compatible UARTs with Send/Receive 16yte FlFOs
  - Supports 230k and 460k Baud Programmable Baud Rate Generator Modem Control Circuitry
  - 480 Address and Eight IRQ Options
- Infrared Port
  - Multiprotocol Infrared Interface
  - 128yte Data FIFO
  - IrDA 1.1 Compliant
  - TEMIC/HP Module Support * Consumer IR
  - SHARP ASK IR
  - 480 Address, Up to Eight IRQ and Three DMA Options
- Multi-mode™ Parallel Port with ChiProtect™
  - Standard Mode IBM PC/XT® PC/AT®, and PS/2™^ Compatible Bidirectional Parallel Port
  - Enhanced Parallel Port {EPP) Compatible EPP 1.7 and EPP 1.9 (IEEE 1284 Compliant)
  - IEEE 1284 Compliant Enhanced Capabilities Port (ECP)
  - ChiProtect Circuitry for Protection Against Damage Due to Printer Power-on
  - 480 Address, Up to Eight IRC1 and Three DMA Options
- ISA Host Interface
  - 16it Address Qualification
  - 8it Data Bus * IOCHRDY for ECP and Fast IR
  - Three 8it DMA Channels
  - Eight Direct Parallel IRQs and Serial IRQ Option Compatible with Serialized IRQ Support for PCI Systems
- 100 Pin OFP and TQFP Package

2.3.2 General Description

The FDC37C67x with Consumer IR and IrDA v 1.1 support incorporates a keyboard interface, SMC's true CMOS 765B floppy disk controller, advanced digital data separator, two 16C550 compatible UARTs, one Multi-Mode parallel port which includes ChiProtect circuitry plus EPP and ECP, on-chip 24 mA AT bus drivers, two floppy direct drive support, Intelligent power management and SMI support. The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures in addition to providing data overflow and underflow protection. The SMC advanced digital data separator incorporates SMC's patented data separator technology, allowing for ease of testing and use. Both on-chip UARTs are compatible with the NS16C550. The parallel port is compatible with IBM PC/AT architecture, as well as IEEE 1284 EPP and ECP. The FDC37C67x incorporates sophisticated power control circuitry (PCC). The PCC supports multiple low power down modes.

The FDC37C67x supports the ISA Plug-and-Play Standard (Version 1.0a) and provides the recommended functionality to support Windows '95. The I/O Address, DMA Channel and Hardware IRQ of each logical device in the FDC37C67x may be reprogrammed through the internal configuration registers. There are 480 I/O address location options, 8 parallel IRQs, an optional Serialized IRQ interface, and three DMA channels.

The FDC37C67x does not require any external filter components and is therefore easy to use and offers lower system costs and reduced board area. The FDC37C67x is software and register compatible with SMC's proprietary 82077AA core

2.3.3 Pin Configuration

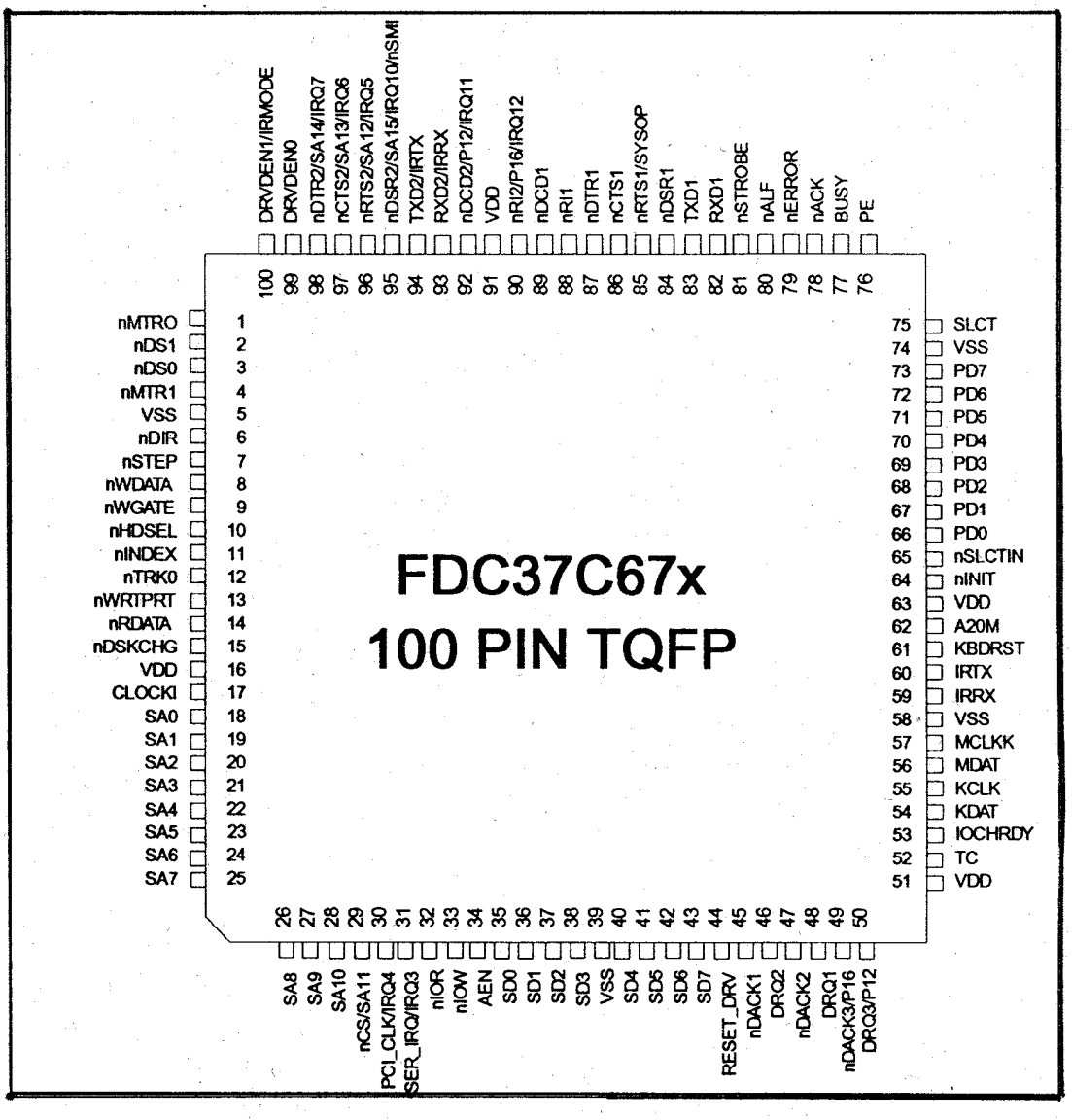


Figure 2-4 FDC37C67 (TQFP) Pin Diagram

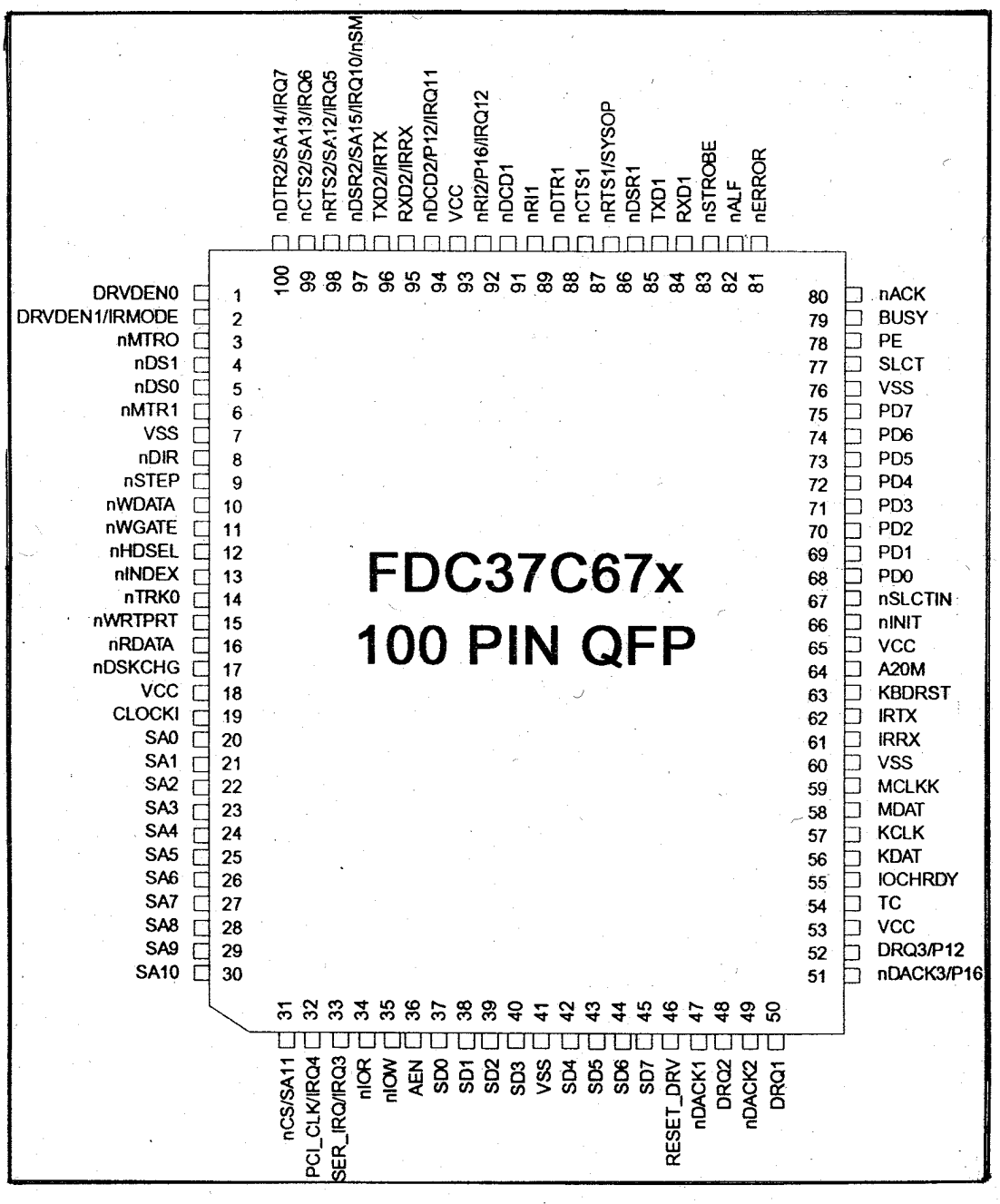


Figure 2-5 FDC37C67 (QFP) Pin Diagram

2.3.4 Pin Descriptions

Table 2-6 FDC37C67 Pin Descriptions

Pin No./QFP	Pin Name	Type	Symbol	Buffer Type
Processor / Host Interface (34)				
E37:40, 42:45	System Data Bus	8	SD[0:7]	IO24
20:30	11-bit System Address Bus	11	SA[0:10]	I
31	Chip select/SA11 (Note 1)	1	nCS/SA11	I
36	Address Enable	1	AEN	I
55	I/O Channel Ready	1	IOCHRDY	OD24
46	ISA Reset Drive	1	RESET_DRV	IS
33	Serial IRQ/Parallel IRQ_3	1	SER_IRQ/IRQ3	IO24/O24/D24(Note 0)
32	PCI Clock for Serial IRQ (33 MHz/30MHz)/Parallel IRQ_4	1	PCI_CLK/IRQ4	IO24/O24/D24(Note 0)
50	DMA Request 1	1	DRQ1	O24
48	DMA Request 2	1	DRQ2	O24
52	DMA Request 3/8042 P12	1	DRQ3/P12	O24/IO24
47	DMA Acknowledge 1	1	nDACK1	I
49	DMA Acknowledge 2	1	nDACK2	I
51	DMA Acknowledge 3/8042 P16	1	nDACK3/P16	I/IO24
54	Terminal Count	1	TC	I
34	I/O Read	1	nIOR	I
35	I/O Write	1	nIOW	I
Clocks(1)				
19	14.318MHz Clock Input	1	CLOCKI	ICLK
Infrared Interface (2)				
61	Infrared Rx	1	IRRX	1
62	Infrared Tx	1	IRTX	O24
Power Pins (8)				
18,53,65,93	Power		VCC	
7,41,60, 76	Ground		VSS	
FDD Interface (16)				
16	Read Disk Data	1	nRDATA	IS
11	Write Gate	1	nWGATE	O224/OD24
10	Write Disk Data	1	nWDATA	O224/OD24
12	Head Select	1	nHDSEL	O224/OD24
8	Step Direction	1	nDIR	O224/OD24
9	Step Pulse	1	nSTEP	O224/OD24
17	D3k _ha_	1	nDSKCHG	IS
5	Dr we 58SM O	1	nDS0	O224/OD24
4	Drive Select 1	1	nDS1	O224/OD24

Table 2-6 FDC37C67 Pin Descriptions

Pin No./QFP	Pin Name	Type	Symbol	Buffer Type
3	Maor On D	1	nMTR0	O224/OD24
6	Motor On 1	1	nMTR1	O224/OD24
15	Write Protected	1	nWRTPRT	IS
14	Track O	1	nTRKO	IS
13	Index Pulse Input	1	nINDEX	IS
1	Drive Density Select O	1	DRVDENO	O224/OD24
2	Drive Density Select 1 /IR Mode Select/IRRX3	1	DRVDEN1/IR MODE/ IRRX3	O224/OD24/O24/I
Serial Port 1 Interface(8)				
84	Receive Serial Data 1	1	RXD1	I
85	Transmit Serial Data 1	1	TXD1	O4
87	Request to Send 1	1	nRTS1/SYSOP	O4/I
88	Clear to Send 1	1	nCTS 1	I
89	Data Terminal Ready 1	1	nDTR 1	O4
86	Data Set Ready 1	1	nDSR 1	I
91	Data Carrier Detect 1	1	nDCD1	I
90	Ring Indicator 1	1	nRI1	I
Serial Port 2 Interface (8)				
95	Receive Serial Data 2/Infrared Rx	1	RXD2/IRRX	I
96	Transmit Serial Data 2/Infrared Tx	1	TXD2/IRTX	O24
98	Request to Send 2/Sys Addr 12/ Parallel IRQ 5	1	nRTS2/SA12/ IRQ5	O4/I/O24/OD24(Note0)
99	Clear to Send 2/Sys Addr 13/ Parallel IRQ 6	1	nCTS2/SA 13/ IRQ6	I/I/O24/OD24(Note0)
100	Data Terminal Ready/Sys Addr 14/ Parallel IRQ 7	1	nDTR2/SA 14/ IRQ7	O4/I/O24/OD24(Note0)
97	Data Set Ready 2/Sys Addr 15/ Parallel IRQ 1 O/nSMI	1	nDSR2/SA1 5/ IRQ10/nSMI	I/I/O24/OD24(Note0)
94	Data Carrier Detect 2/8042 P12/ Parallel IRQ 1 1	1	nDCD2/P12/ IRQ11	I/IO24/O24(Note0)
92	Ring Indicator 2/8042 P1 6/Parallel IRQ 12	1	nRI2/P16/ IRQ12	I/IO24/O24/OD24 (Note0)
Parallel Port Interface {17)				
68:75	Parallel Port Data Bus	8	PD[0:7]	IO24
67	Printer Select	1	nSLCTIN	OD24/O24
66	Initiate Output	1	nlNIT	OD24/O24
82	Auto Line Feed	1	nALF	OD24/O24
83	Strobe Signal	1	nSTROBE	OD24/O24
79	Busy Signal	1	BUSY	I
80	Acknowledge Handshake	1	nACK	I

Table 2-6 FDC37C67 Pin Descriptions

Pin No./QFP	Pin Name	Type	Symbol	Buffer Type
78	Paper End	1	PE	I
77	Printer Selected	1	SLCT	I
81	Error at Printer	1	nERROR	I
Keyboard/Mouse Interface (6)				
56	Keyboard Data .	1	KDAT	IOD16P
57	Keyboard Clock	1	KCLK	IOD16P
58	Mouse Data	1	MDAT	IOD16P
59	Mouse Clock	1	MCLK	IOD16P
63	Keyboard Reset	1	KBDRST(Note 3)	O4
64	Gate A20	1	A20M	O4

Note 0: *The interrupt request is output on one of the IRQx signals as an 024 buffer type. If EPP or ECP Mode is enabled, this output is pulsed low, then released to allow sharing of interrupts. In this case, the buffer type is OD24. Refer to the configuration section for more information.*

Note 1: *For 1 2it addressing, SAO:SA11 only, nCS should be tied to GND. For 1 6it external address qualification, address bits SA11:SA15 can be "ORed" together and applied to nCS. The nCS pin functions as SA11 in full 1 6it Internal Address Qualification Mode.CR24.6 controls the FDC37C67x addressing modes.*

Note 2: *The "n" as the first letter of a signal name indicates an "Active Low" signal.*

Note 3: *KBDRST is active low.*

BUFFER TYPE DESCRIPTIONS

- I Input, TTL compatible.
- IS Input with Schmitt trigger.
- IOD16P Input/Output, 1 6mA sink, 90uA pullup. 0
- IO24 Input/Output, 24mA sink, 1 2mA source.
- IO4 Input/Output, 4mA sink, 2mA source.
- O4 Output, 4mA sink, 2mA source.
- O24 Output, 24mA sink, 1 2mA source.
- OD24 Output, Open Drain, 24mA sink.
- ICLK Clock Input

2.3.5 Description of Multifunction Pins

Table 2-7 FDC37C67 Multifunction Pin Descriptions

Pin No./QFP	Original Function	Alternate Function 1	Alternate Function 2	Default
2	DRVDEN1	IR MODE	IRRX3	DRVDEN1
Controlled by IRMODSEL(LD8:CRC0.0) and IRRX3SEL(LD8:CRC0.4)				
32	PCICLK	IRQ4		PCICLK
33	SERIRQ	IRQ3		SERIRQ
Controlled by SERIRQSEL(LD8:CRCO.2)				
51	nDACK3	8042 P16		nDACK3
52	DRQ3	8042 P12		DRQ3
Controlled by DMA3SEL(LD8:CRCO.1)				
92	nR12	8042 P16	IRQ12	nR12
94	nDCD2	8042 P12	IRQ11	nDCD2
Controlled by 8042COMSEL(LD8:CRCO.3) and SERIRQSEL(LD8:CRCO.2)				
95	RXD2	IRRX		RXD2
96	TXD2	IRTX		TXD2
Controlled by IR Option Register(LD5:CRF1.6)				
97	nDSR2	SA15	IRQ10	nDSR2
98	nRTS2	SA12	IRQ5	nRTS2
99	nCTS2	SA13	IRQ6	nCTS2
100	nDTR2	SA14	IRQ7	nDTR2
Controlled by 16 bit Address Qual.(CR24.6) and SERIRQSEL(LD8:CRC0.2)				

2.3.6 Block Diagram

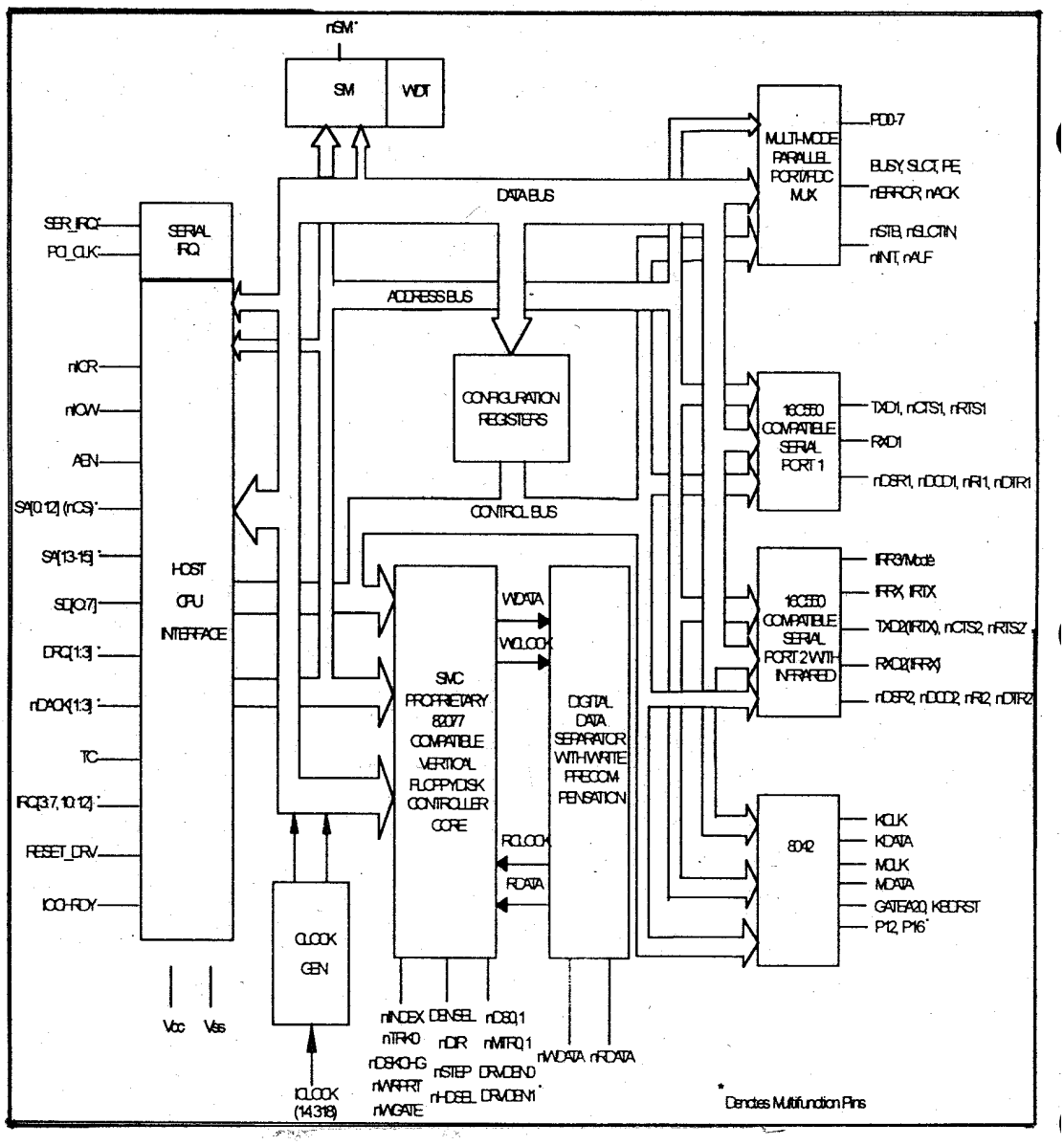


Figure 2-6 FDC37C67 Block Diagram

2.4 65555

2.4.1 Features

- Highly integrated design Flat Panel and CRT GUI Accelerator & Multimedia Engine, Palette/DAC, and Clock Synthesizer
- Hardware Windows Acceleration
  - 64-bit Graphics Engine
    - System-to-Screen and
    - Screen-to-Screen BitBLT
    - 3-Operand Raster-Ops
    - 8/16/24 Color Expansion
  - Transparent BLT
    - Optimized for Windows™ BitBLT format
- PCI Bus with Burst Mode capability and BIOS ROM support
- Flexible Memory Configurations
  - 64-Bit memory interface for EDO
  - Two, four, or eight 256Kx 16 DRAMs (I MB, 2MB, 3MB, or 4MB)
  - One or two 512Kx32 DRAMs (2MB or 4MB)
  - Four 256Kx16 plus two 128Kx32 (3MB)
  - Two 128Kx32 DRAMs (IMB)
  - Four 128Kx16 DRAMs (IMB)
- High Performance:
  - Deep write buffers
- CRT Support
  - 135 MHz RAMDAC
- Hardware Multimedia Support
  - Zoom Video port
  - YUV input from System Bus or Video Port
  - YUV-RGB Conversion
  - Capture / Scaling
  - Video Zoom up to 8x
  - Vertical interpolation of video data up to 720 pixels wide.
  - Double Buffered Video
  - Horizontal Interpolation

- Display centering and stretching features for optimal fit of V(iA graphics and text on 800x600 and 1024x768 panels
- Simultaneous Hardware Cursor and Pop-up Window
  - 64x64 pixels by 4 colors
  - 128x128 pixels by 2 colors
- Game Acceleration
  - Source Transparent BLT
  - Destination Transparent BLT
  - Double buffer support for YUV and 15/16bpp Overlay Engine
  - Instant Full Screen Page Flip
  - Read back of CRT Scan line counters
- Optimized for High-Performance Flat Panel Display at 3.3V
  - 640x480 x 24bpp
  - 800x600 x 24bpp
  - 1024x768 x 24bpp
  - 1280 x 1024 x 24bpp
- 36-bit direct interface to color and monochrome, single drive (SS), and dual drive (DD), STN & TFT panels
- Flexible On-chip Activity Timer facilitates ordered shutdown of the display system
- Advanced Power Management feature minimizes power usage in:
  - Normal operation
  - Standby (Sleep) modes
  - Panel-Off Power-Saving Mode
- VESA Standards supported
  - VAFC Port for display of "Live" Video
  - DPMS for CRT power-down (required for support of EPA Energy-Star program)
  - DDC for CRT Plug-Play & Display Control
- Composite NTSC / PAL Support
  - Flicker Reduction Circuitry
- Power Sequencing control outputs regulate application of bias voltage, +5V to the panel and +12V to the inverter for backlight operation
- 3.3V Operation**,** 5.0V tolerant 1/O
- Fully Compatible with IBM® VGA

2.4.2 Software Support Features

- Drivers Features
  - High Performance Accelerated drivers
  - Compatible across HiQVideo™ family
  - Auto Panning Support
  - LCD/CRT/Simultaneous Mode Support
  - Auto Resolution Change
  - HW Stretching/Scaling
  - Double Buffering
  - Internationalization
  - ChipsCPL (Control Panel Applet)
  - DirectDraw support
  - Games SDK support
  - Dynamic Resolution Switching
  - VGA Graphics applications in Windows
  - VESA DDC extensions
  - VESA DPMS extensions
  - Property Sheet to change Refresh/Display
  - Seamless Windows Support
  - Boot time resolution adjustment
  - DIVE, EnDlVE
  - DCAF
- Multimedia Software
  - Video Port Mana8er for ZV Port
  - PCVideo DLL plus Tuner with DK Board
- Software Utilities
  - DebugVGA
  - Auto testing of all video modes
  - ChipsVGA
  - ChipsEXT
- Software Documentation
  - BIOS OEM Reference Guide
  - Display Driver User's Guide
  - Utilities User's Guide
  - Release Notes for BIOS, Drivers, and Utilities

- Software Support
  - Dedicated Software Applications Engineer
  - BBS Support for Software Updates
- BIOS Features
  - VGA Compatible BIOS
  - PCI Bus Support
  - PnP Support
  - VESA VBE 2.0 (incl. DPMS)
  - DDC 1, DDC 2AB
  - Text and Graphics Expansion
  - Auto Centering
  - 44 (40) K BIOS
  - CRT, LCD, Simultaneous display modes
  - Auto Resolution Switch
  - Multiple Refresh Rates
  - NTSC/PAL support
  - Extended Modes
  - Extended BIOS Functions
  - 1024x768 TFT, DSTN Color Panels
  - Multiple Panel Support (8 panels built in)
  - Get Panel Type Function
  - HW Popup Interface
  - Monitor Detect
  - Pop Up Support
  - SMI and Hot Key support
- System BIOS Hooks
  - Set Active Display Type
  - Save/Restore Video State
  - Setup Memory for Save/Restore
  - SMI Entry Point
  - Int 15 Calls after POST, Set Mode
  - Mixed Voltage 3.3V/5V Support
- BIOS Modify Program (BMP)
  - Clocks
  - Mode support

- Panel Tables
- Voltage Switching
- Int 15 Hooks
- Monitor Sensing

2.4.3 Introduction / Overview

The HiQVideo™ family of high performance multimedia flat panel/CRT GUI accelerators extend CHIPS' offering of high performance flat panel controllers for full-featured notebooks and sub--notebooks. The HiQVideo family offers 64-bit high performance and new hardware multimedia support features.

2.4.3.1 HiQColor™ Technology

The 65555 integrates CHIPS breakthrough HiQColor technology. Based on a new proprietary TMED (Temporal Modulated Energy Distribution) algorithm, HiQColor technology is a unique process that enables the display of 16.7M colors on STN panels without dithering. TMED reduces the need for panel turning associated with current FRC-based algorithms.

Independent of panel response times, the TMED algorithm eliminates all flaws such as shimmer, Mach banding and crawling currently seen on STN panels. Combined with the new fast response high contrast and low-crosstalk technology found in new STN panels. HiQColor technology enables TF^T quality viewing on an STN panel. The 65555 provides the best color fidelity for the widest variety of active and passive panels in the market.

2.4.3.2 Reduced Flicker Output Television

The television output circuitry supports both NTSC and PAL television formats. The 65555 provides filtering circuitry to reduce the flicker circuitry to reduce the flicker seen when displaying CRT resolution images on television screens. The television circuitry scales images to fit both PAL and NTSC televisions.

2.4.3.3 ZV Port Input

The 65555 supports the ZV port PCMCIA standard for video input. The ZV port video data is fed directly to the graphics memory to reduce traffic on the PCI Bus.

2.4.3.4 Hardware Multimedia Support

The HiQVideo™ family uses independent multimedia capture and display systems on-chip. The capture system places data in display memory (usually off screen) and the display system places the data in a window on the screen.

The capture system can receive data from either the system bus or from the ZV enabled video port in either RGB or YUV format. The input data can also be scaled down before storage in display memory. Capture of input data may also be double buffered for smoothing and to prevent image tearing.

The display system can independently place either RGB or YUV data from anywhere in display memory into an on-screen window which can be any size and located at any pixel boundary (YW data is converted to RGB "on-the-fly" on output). Non-rectangular windows are supported via color keying. The data can be fractionally zoomed on output up to 8x to fit the onscreen window and can be horizontally and vertically interpolated. Interlaced and non-interlaced data are supported in both capture and display systems.

2.4.3.5 Video Acceleration

When the system writes to the video YW memory, the 65555 uses its PCI Bust Mode capabilities to allow for a higher frame rate. Video capture input through the ZV port is scaled and stored into memory allowing frame capture for video conferencing. In addition, the 65555 will use vertical interpolation of video data up to 720 pixels wide to enable smooth zooming to full screen MPEG II video. Double buffering is used to prevent image tearing.

2.4.3.6 Versatile Panel Support

The HiQVideo family supports a wide variety of monochrome and color Single-Panel, Single-Drive (SS) and Dual-Panel, Dual Drive (DD) standard and high-resolution passive STN and acfive matrix TFT/MIM LCD, and EL panels. For monochrome panels, up to 64 gray scales are supported. With the help of HiQColor Technology, STN panels can afford 256 gray shades per primary resulting in 16M colors for an improved image representation. Additionally, the HiQVPro also supports TFT panels up to 36-bit interface. The HiQVideo family offers a variety of programmable features to optimize display quality. Vertical centering and stretching are provided for handling modes with less than 480 lines on 480line panels. Horizontal and vertical stretching capabilities are also available for both text and graphics modes for optimal display of VGA text and graphics modes on 800x600 and 1024x768 panels. Three selectable color-to-gray scale reduction techniques and SMARTMAP are available for improving the ability to view color applications on monochrome panels.

2.4.3.7 Low Power Consumption

The HiQVideo family uses a variety of advanced power management features to reduce power consumption of the display sub-system and to extend battery life. Although optimized for 3.3V operation, the HiQVideo controller's internal logic, memory interface, bus interface, and panel interfaces can be independently configured to operate at either 3.3V or 5V.

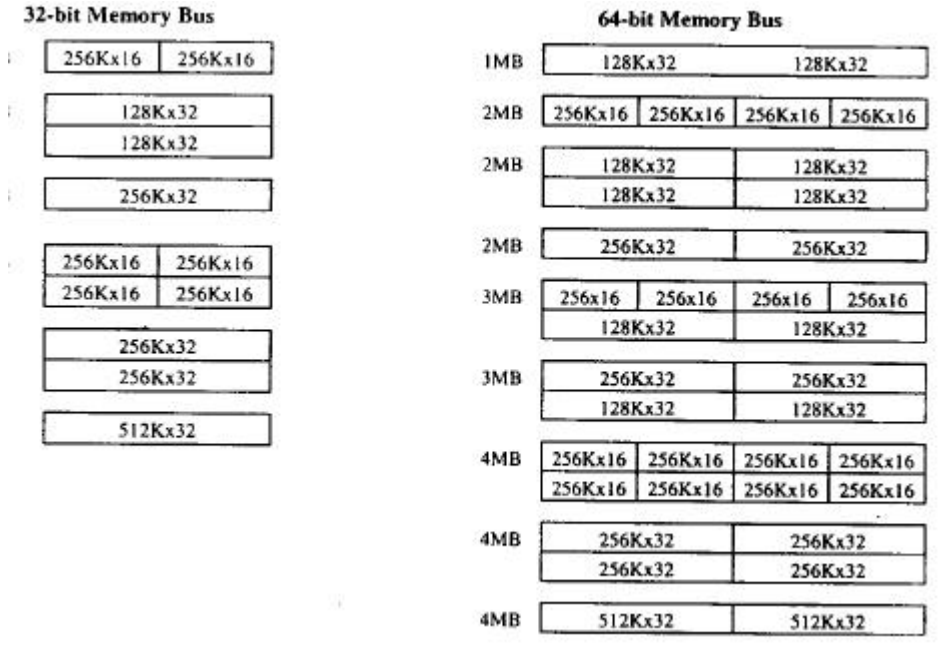
2.4.3.8 Software Compatibility/Flexibility

The HiQVideo controllers are fully compatible with VGA at the register, and BIOS levels. CHIPS and third-party vendors supply fully VGA-compatible BIOS, end-user utilities and drivers for common application programs such as Microsoft Windows and OS/2.

The 65555 BIOS and drivers are an evolutionary step from the 65554 software. The Windows drivers provided for the 65555 are compliant with both Microsoft WHQL and PC97 standards.

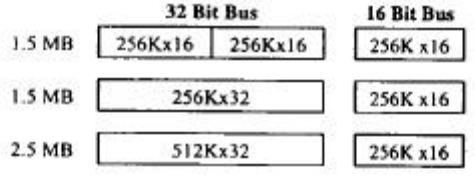
2.4.3.9 Display Memory Size Requirements

The 65555 supports the following 32-bit wide and 64-bit wide memory configuration show below:



The 64-bit wide memory configurations have double the memory bandwidth of the 32-bit wide configurations.

The figure below shows the display memory configurations using and external STN-DD buffer:



- *Some of the 32-bit configurations allow an additional 256K x 16 device to be used for an external 16-bit wide STN-DD buffer, as shown above.*
- *The 65555 supports both video capture/playback and external STN-DD buffer at the same time*

2.4.4 Pin Descriptions

2.4.4.1 Introduction

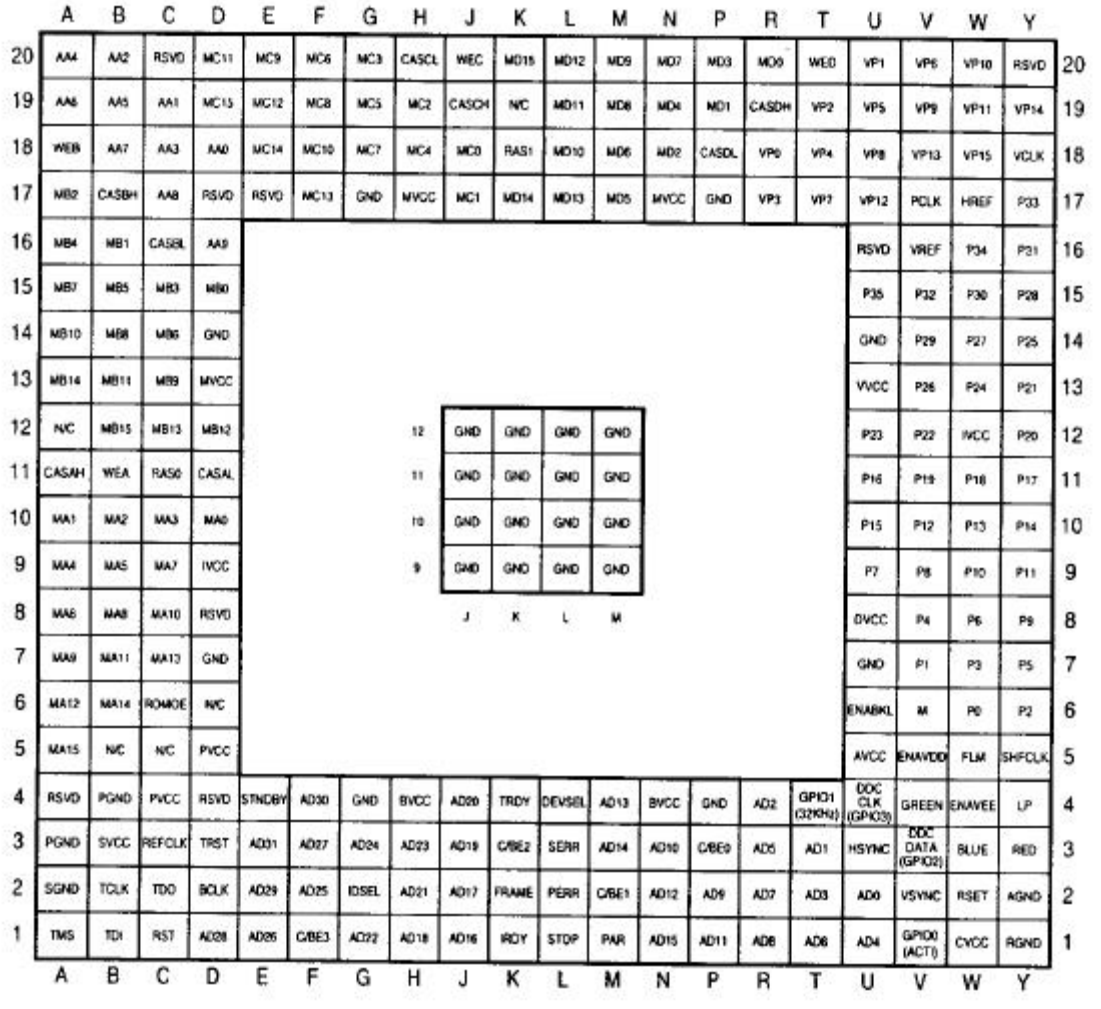
The following pages contain the BGA ball assignments and a list of all the pins for the 65555 GUI Accelerator. The pins are divided into the following groups:

- PCI Bus

- Display Memory Interface
- Flat Panel Display Interface
- CRT Interface Power / Ground and Standby Control
- Video Interface; Miscellaneous

Pin name in parentheses(...) indicate alternate functions.

2.4.4.2 Top View: BGA Ball Assignments

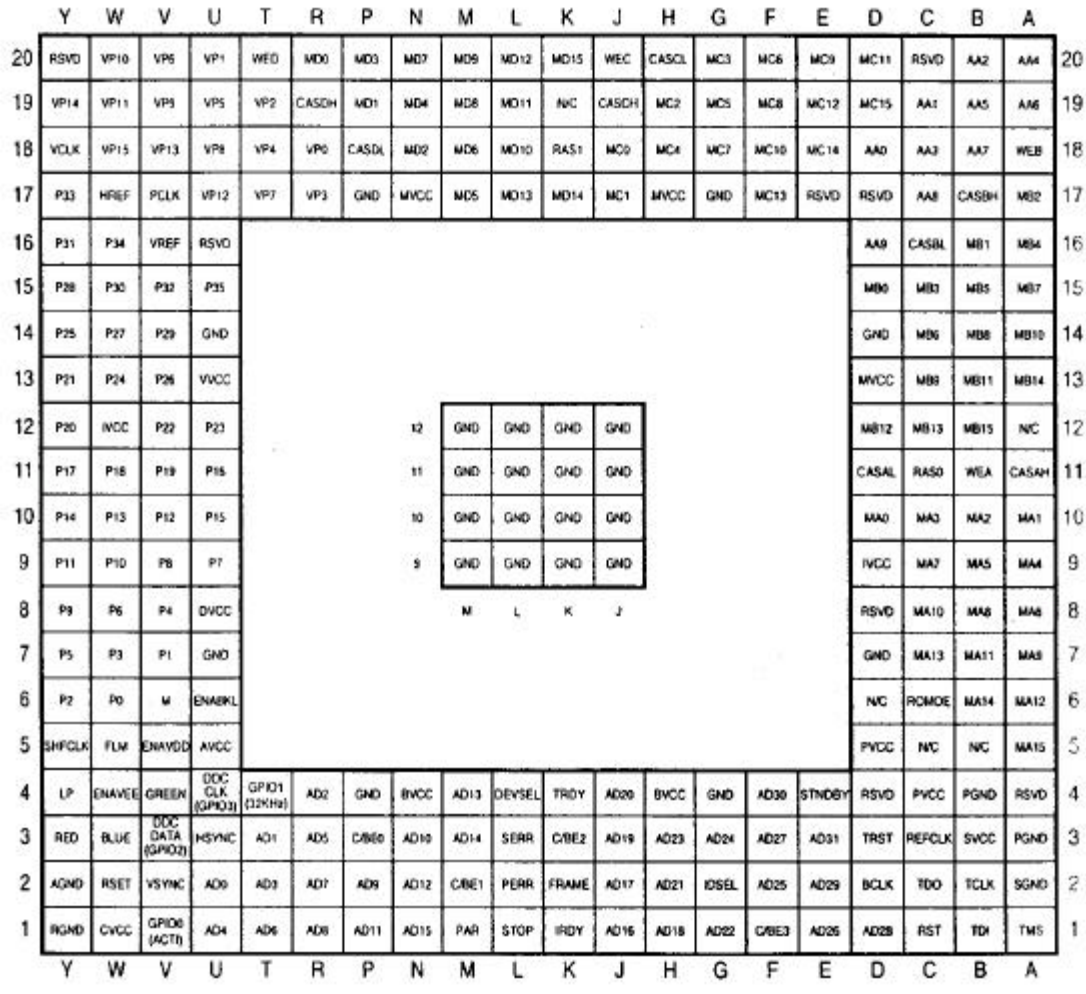


	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	
20	AA4	AA2	RSVD	MC11	MC9	MC6	MC3	CASCL	WEC	MD15	MD12	MD9	MD7	MD3	MD0	WE0	VP1	VP6	VP10	RSVD	20
19	AA6	AA5	AA1	MC15	MC12	MC8	MC5	MC2	CASCH	N/C	MD11	MD8	MD4	MD1	CASDH	VP2	VP5	VP9	VP11	VP14	19
18	WEB	AA7	AA3	AA0	MC14	MC10	MC7	MC4	MC0	RAS1	MD10	MD6	MD2	CASDL	VP0	VP4	VP8	VP13	VP15	VCLK	18
17	MB2	CASBH	AA8	RSVD	RSVD	MC13	GND	MVCC	MC1	MD14	MD13	MD5	MVCC	GND	VP3	VP7	VP12	PCLK	HREF	P33	17
16	MB4	MB1	CASBL	AA9													RSVD	VREF	P34	P31	16
15	MB7	MB5	MB3	MB0													P35	P32	P30	P28	15
14	MB10	MB8	MB6	GND													GND	P29	P27	P25	14
13	MB14	MB11	MB9	MVCC													VVCC	P26	P24	P21	13
12	N/C	MB15	MB13	MB12				12	GND	GND	GND	GND					P23	P22	IVCC	P20	12
11	CASAH	WEA	RAS0	CASAL				11	GND	GND	GND	GND					P16	P19	P18	P17	11
10	MA1	MA2	MA3	MA0				10	GND	GND	GND	GND					P15	P12	P13	P14	10
9	MA4	MA5	MA7	IVCC				9	GND	GND	GND	GND					P7	P8	P10	P11	9
8	MA6	MA8	MA10	RSVD					J	K	L	M					DVCC	P4	P6	P9	8
7	MA9	MA11	MA13	GND													GND	P1	P3	P5	7
6	MA12	MA14	ROMOE	N/C													ENABKL	M	P0	P2	6
5	MA15	N/C	N/C	PVCC													AVCC	ENAVDD	FLM	SHFCLK	5
4	RSVD	PGND	PVCC	RSVD	STNDBY	AD30	GND	BVCC	AD29	TRDY	DEVSEL	AD13	BVCC	GND	AD2	GPIO1 (32KHz)	DDC CLK (GPIO3)	GREEN	ENAVEE	LP	4
3	PGND	SVCC	REFCLK	TRST	AD31	AD27	AD24	AD23	AD19	C/BE2	SERR	AD14	AD10	C/BE0	AD5	AD1	HSYNC	DDC DATA (GPIO2)	BLUE	RED	3
2	SGND	TCLK	TDO	BCLK	AD29	AD25	IDSEL	AD21	AD17	FRAME	PERR	C/BE1	AD12	AD9	AD7	AD3	AD0	VSYNC	RSET	AGND	2
1	TMS	TDI	RST	AD28	AD26	C/BE3	AD22	AD18	AD16	IRDY	STOP	PAR	AD15	AD11	AD8	AD6	AD4	GPIO0 (ACT)	CVCC	RGND	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	

Note: Balls D5 and C4 (PVCC) may be jumpered together
Balls B4 and A3 (PGND) may be jumpered together

Figure 2-7 65555 BGA Ball Assignments (Top View)

2.4.4.3 Bottom View: BGA Ball Assignments



	Y	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
20	RSVD	VP10	VP6	VP1	WED	MD0	MD3	MD7	MD9	MD12	MD15	WEC	CASCL	MC3	MC6	MC9	MC11	RSVD	AA2	AA4	20
19	VP14	VP11	VP5	VP5	VP2	CASDH	MD1	MD4	MD8	MD11	N/C	CASCH	MC2	MC5	MC8	MC12	MC15	AA1	AA5	AA6	19
18	VCLK	VP15	VP13	VP8	VP4	VP0	CASDL	MD2	MD6	MD10	RAS1	MC0	MC4	MC7	MC10	MC14	AA0	AA3	AA7	WEB	18
17	P33	HREF	PCLK	VP12	VP7	VP3	GND	MVCC	MD5	MD13	MD14	MC1	MVCC	GND	MC13	RSVD	RSVD	AA8	CASBH	MB2	17
16	P31	P34	VREF	RSVD													AA9	CASBL	MB1	MB4	16
15	P28	P30	P32	P35													MB0	MB3	MB5	MB7	15
14	P25	P27	P29	GND													GND	MB6	MB8	MB10	14
13	P21	P24	P26	VVCC													MVCC	MB8	MB11	MB14	13
12	P20	IVCC	P22	P23				12	GND	GND	GND	GND					MB12	MB13	MB15	N/C	12
11	P17	P18	P19	P16				11	GND	GND	GND	GND					CASAL	RAS0	WEA	CASAH	11
10	P14	P13	P12	P15				10	GND	GND	GND	GND					MA0	MA3	MA2	MA1	10
9	P11	P10	P8	P7				9	GND	GND	GND	GND					IVCC	MA7	MA5	MA4	9
8	P9	P6	P4	DVCC					M	L	K	J					RSVD	MA10	MA6	MA8	8
7	P5	P3	P1	GND													GND	MA13	MA11	MA9	7
6	P2	P0	M	ENABKL													N/C	ROMOE	MA14	MA12	6
5	SHFCLK	FLM	ENAVDD	AVCC													PVCC	N/C	N/C	MA15	5
4	LP	ENAVEE	GREEN	DDC CLK (GPIO3)	GPIO1 (32KHz)	AD2	GND	BVCC	AD13	DEVSEL	TRDY	AD20	BVCC	GND	AD30	STNDBY	RSVD	PVCC	PGND	RSVD	4
3	RED	BLUE	DDC DATA (GPIO2)	HSYNC	AD1	AD5	C/BE0	AD10	AD14	SERR	C/BE2	AD19	AD23	AD24	AD27	AD31	TRST	REFCLK	SVCC	PGND	3
2	AGND	RSET	VSYNC	AD0	AD3	AD7	AD9	AD12	C/BE1	PERR	FRAME	AD17	AD21	IDSEL	AD25	AD29	BCLK	TDO	TCLK	SGND	2
1	RGND	CVCC	GPIO0 (ACTI)	AD4	AD6	AD8	AD11	AD15	PAR	STOP	IRDY	AD16	AD18	AD22	C/BE3	AD26	AD28	RST	TDI	TMS	1
	Y	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	

Figure 2-8 65555 BGA Ball Assignments (Bottom View)

2.4.4.4 Pin Functions

Table 2-8 65555 Pin Functions

Ball	Pin Name	Type	Active	Description
PCI Bus Interface				
C1	RST#	In	Low	Reset. This input sets all signals and registers in the chip to a known slate. All outputs from the chip are tri-stated or driven to an inactive state. **This pin is ignored during Standby mode (STNDBY# pin low). The remainder of the system (therefore the system bus) may be powered down if desired (all bus output pins are tri-stated in Standby mode).**
D2	BCLK	In	High	Bus Clock. This input provides the timing reference for all PCI bus transactions. All bus inputs except RESET# are sampled on the rising edge of BCLK. BCLK may be any frequency from DC to 33MHz.
M1	PAR	I/O	High	Parity. This signal is used to maintain even parity across AD031 and C/BE0-3#. PAR is stable and valid one clock after the address phase. For data phases PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase (i.e., PAR has the same timing as AD0-3I but delayed by one clock). The bus master drives PAR for address and write data phases; the target drives PAR for read data phases.
K2	FRAME#	In	Low	Cycle Frame. Driven by the current master to indicate the beginning and duration of an access. Assertion indicates a bus transaction is beginning (while asserted, data transfers continue); de-assertion indicates the transaction is in the final data phase
K1	IRDY#	In	Low	Initiator Ready. Indicates the bus master's ability to complete the current data phase of the transaction. During a write, IRDY# indicates valid data is present on AD0-3 1; during a read it indicates the master is prepared to accept data. A data phase is completed on any clock when both IRDY# and TRDY# are sampled then asserted (wait cycles are inserted until this occurs).
K4	TRDY#	S/TS	Low	Target Ready. Indicates the target's ability to complete the current data phase of the transaction. During a read, TRDY# indicates that valid data is present on AD0-3 1; during a write it indicates the target is prepared to accept data. A data phase is completed on any clock when both IRDY# and TRDY# are sampled then asserted (wait cycles are inserted until this occurs).
L1	STOP#	S/TS	Low	Stop. Indicates the current target is requesting the master to stop the current transaction.

Table 2-8 65555 Pin Functions

Ball	Pin Name	Type	Active	Description
L4	DEVSEL#	S/TS	Low	Device Select. Indicates the current target has decoded its address as the target of the current access
L2	PERR#	S/TS	Low	Parity Error. This signal reports data parity errors (except for Special Cycles where SERR# is used). The PERR# pin is Sustained Tri-state. The receiving agent will drive PERR# active two clocks after detecting a data parity error PERR# will be driven high for one clock before being tri-stated as with all sustained tri state signals. PERR# will not report status until the chip has claimed the access by asserting DEVSEL# and completing the data phase.
L3	SERR#	OD	Low	System Error. Used to report system errors where the result will be catastrophic (address panty error, data panty errors for Special Cycle commands, etc.). This output is actively driven for a single PCI clock cycle synchronous to BCLK and meets (he same setup and hold time requirements as all other bused signals. SERR# is not driven high by the chip after being asserted, but is pulled high only by a weak pull-up provided by the system. Thus, SERR# on the PCI bus may take two or three clock periods to fully return to an inactive state.

Note: *S/TS stands for "Sustained Tri-state". These signals are driven by only one device at a time, are driven high for one clock before released, and are not driven for at least one cycle after being released by the previous device. A pull-up provided by the bus controller is used to maintain an inactive level between transactions.*

All signals listed above are powered by BVCC and GND. ROMOE# is powered by MVCC and GND.

Table 2-8 65555 Pin Functions

Ball	Pin Name	Type	Active	Description
U2 T3 R4 T2 U1 R3 T1 R2 R1 P2 N3 P1 N2 M4 M3 N1 J1 J2 H1 J3 J4 H2 G1 H3 G3 F2 E1 F3 D1 E2 F4 E3	AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	High High High High High High High High High High High High High High High High High High High High High High High High High High High High High High High	PCI Address/Data Bus Address and data are multiplexed on the same pins. A bus transaction consists of an address phase followed by one or more data phases (both read and write bursts are allowed by the bus definition). The address phase is the clock cycle in which FRAME# is asserted (AD0-31 contain a 32-bit physical address) For l/O, the address is a byte address. For memory and configuration, the address is a DWORD address. During data phases AD0-7 contain the LSB and 24-31 contain the MSB. Write data is stable and valid when IRDY# is asserted; read data is stable and valid when TRDY# is asserted. Data transfers only during those clocks when both IRDY# and TRDY# are asserted. **C/BE3-0 Command Type Support** 0000 Interrupt Acknowledge 0001 Special Cycle 0010 I/O Read Y 0011 I/O Write Y 0100 -reserved- 0101 -reserved- 0110 Memory Read Y 0111 Memory Write Y 1000 -reserved 1001 -reserved- 1010 Configuration Read Y 1011 Configuration Write Y 1100 Memory read Multiple 1101 Dual Address Cycle 1110 Memory Read Line 1111 Memory Read & Invalidate
P3 M2 K3 F1	C/BE0# C/BE1# C/BE2# C/BE3#	In In In in	Low Low Low Low	Bus Command/Byte Enables. During the address phase of a bus transaction, these pins define the bus command (see list above). During the data phase, these pins are byte enables that determine which byte lanes carry meaningful data: byte 0 corresponds to AD07, byte 1 to 8-15, byte 2 to 16-23. and byte 3 to 2431
G2	IDSEL	In	High	Initialization Device Select. Used as a chip select during configuration read and write transactions
Note: *All signals listed above are powered by BVCC and GND.*				

Table 2-8 65555 Pin Functions

Ball	Pin Name	Type	Active	Description
Display Memory Interface				
D18 CI9 B20 C18 A20 BI9 AI9 B18 C17 D16	AA0 (CFG0) AAI (CFG1) AA2 (CFG2) AA3 (CFG3) AA4 (CFG4) AA5 (CFG5) AA6 (CFG6) AA7 (CFG7) AA8 (CFG8) AA9 (CFG9)	I/O I/O I/O I/O I/O I/0 I/O I/O I/O I/O	Both Both Both Both Both Both Both Both Both Both	DRAM address bus for Bank 0 and Bank AA0 through AA9 also serve as configuration bits CFG0 through CFG9. Please see the descriptions for registers XR70 and XR71 for complete details on configuration
D10 A10 B10 C10 A9 B9 A8 C9 B8 A7 C8 B7 A6 C7 B6 A5	MA0 (TM0) MA1 (TM1) MA2 (CFG10) MA3 (CFG11) MA4 (CFG12) MA5 (CFG13) MA6 (CFG14) MA7 (CFG15) MA8 (RMD0) MA9 (RMDI) MA10 (RMD2) MA11 (RMD3) MA12 (RMD4) MA13 (RMD5) MA14 (RMD6) MA15 (RMD7)	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	High High High High High High High High High High High High High High High High	DRAM data bits 0-15. MA0 is also a test mode signal (Tri-Stale Enable). MA1 is also a test mode signal (ICT Enable). MA2 through MA7 also serve as configuration bits CFG10 through CFG15. Please see the description for register XR71 for complete details on configuration options. MA8 through MA15 are also serve as the data bus for the BIOS ROM during system startup (i.e., before the system enables the graphics controller memory interface).
D15 B16 A17 C15 A16 B15 C14 A15 B14 C13 A14 B13 D12 C12 A13 B12	MB0 (RMA0) MBI (RMAI) MB2 (RMA2) MB3 (RMA3) MB4 (RMA4) MB5 (RMA5) MB6 (RMA6) MB7 (RMA7) MB8 (RMA8) MB9 (RMA9) MB10 (RMA10) MB11 (RMA11) MB12 (RMA12) MB13 (RMA13) MB14 (RMA14) MB15 (RMA15)	I/0 I/O I/O I/O I/O I/O I/O I/O I/O I/0 I/O I/O I/O I/O I/O I/O	High High High High High High High High High High High High High High High High	DRAM data bits 16-31. MB0 through MB15, along with MDI I and MD12, also serve as the address bus for the BIOS ROM during startup (i.e., before he system enables the graphics controller memory interface). Normally, a separate graphics BIOS ROM is not required in portable computer designs, because the graphics BIOS is normally placed in the same ROM devices as the system BIOS. However, this graphics controller provides this BIOS ROM interface capability for use in development systems and add-in cards for flat panel displays. Since the PCI bus specification requires only one load on the PCI bus for each PCI device, this BIOS ROM interface is provided to allow access to the BIOS ROM through the graphics controller chip, itself.

Table 2-8 65555 Pin Functions

Ball	Pin Name	Type	Active	Description
J18 J17 H19 G20 H18 G19 F20 G18 F19 D20 E19 F17 E18 D19	MC0 MC1 MC2 MC3 MC4 MC5 MC6 MC7 MC8 MC11 MC12 MC13 MC14 MC15	I/0 I/O I/O I/O I/O I/O I/O I/O I/O I/0 I/O I/O I/O I/O	High High High High High High High High High High High High High High	DRAM data bits 32-47.
R20 P19 N18 P20 N19 M17 M18 N20 M19 M20 L18 L19 L20 L17 K17 K20	MD0 MD1 MD2 MD3 MD4 MD5 MD6 MD7 MD8 MD9 MD10 MD11(RMA16) MD12(rma17) MD13 MD14 MD15	I/0 I/O I/O I/O I/O I/O I/O I/O I/O I/0 I/O I/O I/O I/O I/O I/O	High High High High High High High High High High High High High High High High	DRAM data bits 48-63. MD11-12 are also ROM addresses 16-17. MD11 and MD12, along with MB0 through MB15, also serve as the address bus for the BIOS ROM during startup (i.e., beore the system enables the graphics controller memory interface).
C11 K18#	RAS0# PAS1#	Out Out	Low Low	RAS for DRAM Bank 0 (128K, 256K, or 512K by 64-bit). RAS for DRAM Bank 1.
C6	ROMOE#(MCLKOUT)	Out	Low	Output Enable for BIOS ROM. May be configured as MCLK output in test mode.
D11 A11 C16 B17 H20 J19 P18 R19	ASAL# ASAH# CASBL# CASBH# ASCL# ASCH# ASDL# CASH#	Out Out Out Out Out Out Out Out	High High High High High High High High	CAS for dual-CAS EDO DRAM. Memory data byte mask signals. one mask signal for each of the eight data bytes in the 64-bit Qword. The masking is performed on a per-byte basis. A given byte is masked when the signal is high, or enabled when the signal is low. Masking is needed on write operations to specify which bytes in the 64-bit word are being written.
B11	WEA#	Out	Low	MA[15:0] write enable for dual-CAS EDO DRAM
A18	WEB#	Out	Low	MB[15:0] write enable for dual-CAS EDO DRAM
J20	WEC#	Out	Low	MC[15:0] write enable for dual-CAS EDO DRAM
T20	WED#	Out	Low	MD[15:0] write enable for dual-CAS EDO DRAM

Note: *All signals listed above are powered by MVCC and GND.*

The 8 bytes comprising each 64-bit Qword are labeled AL, AH, BL, BH, CL, CH, DL, and DH. There is a separate byte mask signal for each byte. Up to two banks can be supported, with RAS0# controlling the first bank and RAS l# controlling the second bank. The address, data and byte mask signals are the same for each bank.

Table 2-8 65555 Pin Functions

Ball	Pin Name	Type	Active	Description
Flat Panel Display Interface				
W6	P0	Out	High	Flat panel data bus of up to 36-bits
V7	P1	Out	High	
Y6	P2	Out	High	
W7	P3	Out	High	
V8	P4	Out	High	
Y7	P5	Out	High	
W8	P6	Out	High	
U9	P7	Out	High	
V9	P8	Out	High	
Y8	P9	Out	High	
W9	P10	Out	High	
Y9	P11	Out	High	
V10	P12	Out	High	
W10	P13	Out	High	
Y10	P14	Out	High	
U10	P15	Out	High	
U11	P16	Out	High	
Y11	P17	Out	High	
W11	P18	Out	High	
V11	P19	Out	High	
Y12	P20	Out	High	
Y13	P21	Out	High	
V12	P22	Out	High	
U12	P23	Out	High	
W13	P24	Out	High	
Y14	P25	Out	High	
V13	P26	Out	High	
W14	P27	Out	High	
Y15	P28	Out	High	
V14	P29	Out	High	
W15	P30	Out	High	
Y16	P31	Out	High	
V15	P32	Out	High	
Y17	P33	Out	High	
W16	P34	Out	High	
U15	P35	Out	High	
Y5	SHFCLK	Out	High	Shift Clock. Pixel clock for nat panel data
W5	FLM	Out	High	First Line Marker. Flat Panel equivalent of VSYNC
Y4	LP (CL1)(DE)(BLANK#)	Out	High	Latch Pulse (may also be called CL1). Flat Panel equivalent of HSYNC. May also be configured as DE (display enable) or BLANK# output
V6	M (DE)(BLANK#)	Out	High	M signal for panel AC drive control (may also be called ACDCLK). May also be configured as DE (display enable) or BLANK# output
V5	ENAVDD	I/O	high	Power sequencing control for panel driver electronics voltage VDD
W4	ENAVEE(ENABKL)	I/O	High	Power sequencing control for panel bias voltage VEE. May also be configured as ENABKL
U6	ENABKL	I/O	High	Power sequencing control for enabling the backlight.

Table 2-8 65555 Pin Functions

Ball	Pin Name	Type	Active	Description
Note: *All signals listed above are powered by DVCC and GND.*				

Notes for table below:

- *To accommodate a wide variety of panel types, the graphics controller has been designed to output its data in any of a number of formats. These formats include different data widths for the colors belonging to each pixel, and the ability to accommodate different pixel data transfer timing requirements.*
- *For STN-DD panels, pins PO through P35 are organized into groups corresponding to the upper and lower parts of the panel. The names of the signals for the upper and lower parts follow a naming convention of Uxx and Lxx, respectively.*
- *For panels that require a pair of adjacent pixels be sent with every shift clock, pins PO through P35 are organized into groups corresponding to the first and second (from right to left) pixels of each pair of pixels being sent. The names of the signals for the first and second pixels of each such pair follow a naming convention of Fxx and Sxx, respectively.*
- *Panels that transfer data on both edges of SHFCLK are also supported. See the description for register FR12 for more details.*

Pin#	Pin Name	Mono SS 8-bit	Mono DD 8=bit	Mono DD 16 bit	Color TFT 9/12/16bit	Color TFT 18/24 bit	Color TFT 36 bit	Color TFT HR 18/24 bit	Color STN SS 8-it(4bP)	Color STN SS 8-bit(4bp)	Color STN DD 8-bit(4bp)	Color STN DD 8-bit(4bp)	Color STN DD 8-bit
W6	P0	P0	UD3	UD7	B0	B0	FB0	FB0	R1	R1	UR1	UR0	UR0
V7	P1	P1	UD2	UD6	B1	B1	FB1	B1	B1	G1	UG1	UG0	UG0
Y6	P2	P2	UD1	UD5	B2	B2	FB2	FB2	G2	B1	UB1	UB0	UB0
W7	P3	P3	UD0	UD4	B3	B3	FB3	FB3	R3	R2	UR2	UR1	LR0
V8	P4	P4	LD3	UD3	B4	B4	FB4	SB0	B3	G2	LR1	LR0	LG0
Y7	P5	P5	LD2	UD2	G0	B5	FB5	SB1	G4	B2	LG1	LG0	LB0
W8	P6	P6	LD1	UD1	G1	B6	SB0	SB2	R5	R3	LB1	LB0	UR1
U9	P7	P7	LD0	LD0	G2	B7	SB1	SB3	B5	G3	LR2	LR1	UG1
V9	P8	-	-	LD7	G3	G0	SB2	FG0	-	B3	-	UG1	UB1
Y8	P9	-	-	LD6	G4	G1	SB3	FG1	-	R4	-	UB1	LR1
W9	P10	-	-	LD5	G5	G2	SB4	FG2	-	G4	-	UR2	LG1
Y9	P11	-	-	LD4	R0	G3	SB5	FG3	-	B4	-	UG2	LB1
V10	P12	-	-	LD3	R1	G4	FG0	SG0	-	R5	-	LG1	UR2
W10	P13	-	-	LD2	R2	G5	FG1	SG1	-	G5	-	LB1	UG2
Y10	P14	-	-	LD1	R3	G6	FG2	SG2	-	B5	-	LR2	UB2
U10	P15	-	-	LD0	R4	G7	FG3	SG3	-	R6	-	LG2	LR2
U11	P16	-	-	-	-	R0	FG4	FR0	-	-	-	-	LG2
Y11	P17	-	-	-	-	R1	FG5	FR1	-	-	-	-	LB2
W11	P18	-		-	-	R2	SG0	FR2	-	-	-	-	UR3
V11	P19	-	-	-	-	R3	SG1	FR3	-	-	-	-	UG3
Y12	P20	-	-	-	-	R4	SG2	SR0	-	-	-		UB3
Y13	P21	-	-	-	-	R5	SG3	SR1	-	-	-	-	LR3
V12	P22	-	-	-	-	R6	SG4	SR2	-	-	-	-	LG3
U12	P23	-	-	-	-	R7	SG5	SR3	-	-	-	-	LB3
W13	P24	-	-	-	-	-	FR0	-	-	-	-	-	-
Y14	P25	-	-	-	-	-	FR1	-	-	-	-	-	-
V13	P26	-	-	-	-	-	FR2	-	-	-	-	-	-
W14	P27	-	-	-	-	-	FR3	-	-	-	-	-	-
Y15	P28	-	-	-	-	-	FR4	-	-	-	-	-	-
V14	P29	-	-	-	-	-	FR5	-	-	-	-	-	-
W15	P30	-	-	-	-	-	SR0	-	-	-	-	-	-
Y16	P31	-	-	-	-	-	SR1	-	-	-	-	-	-
V15	P32	-	-	-	-	-	SR2	-	-	-	-	-	-
Y17	P33	-	-	-	-	-	SR3	-	-	-	-	-	-
W16	P34	-	-	-	-	-	SR4	-	-	-	-	-	-
U15	P35	-	-	-	-	-	SR5	-	-	-	-	-	-
Y15	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK
Pixels/Clock:		8	8	16	1	1	2	2	2-2/3	5-1/3	2-2/3	5-1/3	8

Table 2-8 65555 Pin Functions (continued)

Ball	Pin Name	Type	Active	Description
CRT Interface				
U3	HYSNC(CSYNC)	Out	Both	CRT Horizontal Sync (polarity is programmable) or "Composite Sync" for support of various external NTSC/PAL encoder chips
V2	VSYNC	Out	Both	CRT Vertical Sync (polarity is programmable)
Y3 V4 W3	RED GREEN BLUE	Out Out Out	Analog Analog Analog	CRT analog video outputs from the internal color palette DAC. The DAC is designed for a 37.5S2 equivalent load on each pin (e.g. 75Q resistor on the board, in parallel with the 75D CRT load)
W2	RSET	In	N/A	Set point resistor for the internal color palette DAC. A 560 Q 1% resistor is required between RSET and AGND
V3 U4	DDC DATA(GPIO2) DDC CLK(GPIO3)	I/O I/O	High High	General purpose I/0, suitable for use as DDC data. General purpose I/0, suitable for use as DDC DATA. These two pins are functionally suitable for a DDC interface between the 65555 and a CRT monitor
Note: *HSYNC, VSYNC, GPIO2, and gpio3 are powered by CVCC and GND. RED, GREEN, BLUE and RSET are powered by AVCC and AGND.*				
Power/Ground and Standby Control				
U5	AVCC	VCC	-	Analog power and ground pins for noise isolation for the internal color palette DAC. AVCC should be isolated from digital VCC as described in the Functional Description of the internal color palette DAC. For proper DAC operation, AVCC should not be greater than IVCC. AGND should be common with digital ground but must be lightly decoupled to AVCC. See the Functional Description of the internal color palette DAC for further information
B3 A2 C4,D5 A3, B4 W1	SVCC SGND PVCC PGND CVCC	VCC GND VCC GND VCC	- - - 	Analog power and ground pins for noise isolation for the internal clock synthesizer (for MCLK). Must be the same as IVCC, 3.3V. Analog power and ground pins for noise isolation for internal clock synthesizer (for VCLK). Must be the same as IVCC. SVCC/SGND and PVCC/PGND pairs must be carefully decoupled individually. Refer also lo the section on clock ground layout in the Functional Description. Power for CRT Interface, 3.3V.
D9, & W12 D14 D7 G17 G4, P17	IVCC GND	VCC GND	- -	Power/Ground (Internal Logic), 3.3V. Note that this voltage must be the same as SVCC and PVCC (voltages for internal clock synthesizers)

Table 2-8 65555 Pin Functions (continued)

Ball	Pin Name	Type	Active	Description
P4, U14, U7, J9-12 K9-12 L9-12 M9-12 Y1	RGND	GND		Internal reference GND, should be tied to GND
H4,N4	BVCC	VCC	-	Power (Bus Interface), 3.3V
U8	DVCC	VCC	-	Power (Flat Panel Interface), 3.3V
D13 H17 N17	MVCC	VCC	-	Power (Memory Interface), 3.3V.
U13	VVCC	VCC	-	Power (Video Interface), 3.3V.
Video Interface				
V16	VREF	I/O	High	Vertical reference input for video data port.
W17	HREF	In	High	Horizontal reference input for video data port
Y18	VCLK	In	High	Clock input for video data port.
V17	PCLK(VCLKOUT)	Out	High	Outputs DCLK, or DCLK divided by 2. See the description for register XR60 for complete details. Usable with either the video data port or the flat panel interface. May also be configured to output VCLK in test mode.
R18 U20 T19 R17 T18 U19 V20 T17 U18 V19 W20 W19 U17 V18 Y19 V18	VP0 VP1 VP2 VP3 VP4 VP5 VP6 VP7 VP8 VP9 VP10 VP11 VP12 VP13 VP14 VP15	In In In In In In In In In In In In In In In In	High High High High High High High High High High High High High High High High	Data bus for video data port. When used as a ZV-Port interface, VP0-7 correspond to Y0-7, and VP8-15 correspond to UV0-7.
Note: *All signals listed above are powered by VVCC and GND.*				
Boundary Scan				
A1	TMS	In	High	Test mode select for boundary scan
B2	TCLK(DCLKIN)	In	High	Test clock for boundary scan. Can be configured to be used as an input for an externally provided DCLK through a strapping option. See the descriptions for registers XR70 and XRCF for complete details

Table 2-8 65555 Pin Functions (continued)

Ball	Pin Name	Type	Active	Description
B1	TD1(MCLKIN)	In	High	Test data input for boundary scan. Can be configured to be used as an input for an externally provided MCLK through a strapping option and register programming. See the descriptions for registers XR70 and XRCF for complete details
C2	TDO	In	High	Test data out for boundary scan.
D3	TRST#	In	High	Test reset for boundary scan.
Note: *TMS, TCLK, TDI, TDO and TRST#, are powered by BVCC and GND.*				
Miscellaneous				
E4	STNDBT#	In	Low	Standby Control Pin. Pull this pin low to place the chip in Standby Mode. A low to high transition on the pin will cause change to exit standby mode, host standby mode. and panel off mode.
C3	REFCLK(MCLKIN)	In	High	Reference Clock Input. This pin serves as the input for an external reference oscillator (usually 14.31818 MHz). All timings of the 65555 are derived from this primary clock input source. Can be configured to be used as an input for an externally provided MCLK through a strapping option and register programming. For normal operation. TDI should be used as the input for an externally provided MCLK
V1	GPIO0(ACTI)	I/O	High	General Purpose l/O pin, or ACTI (Activity Indicator).
T4	GPIO1(32KHz)	I/O	High	General Purpose l/O pin, or 32KHz input: clock input for refresh of non-self-refresh DRAMs and panel power sequencing
D6 C5 A12 K19	N/C N/C N/C N/C	n/a n/a n/a n/a	n/a n/a n/a n/a	These pins should be left open.
Y20 D8 D17 A4 B5 D4 U16 C20 E17	Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved	n/a n/a n/a n/a n/a n/a n/a n/a n/a	n/a n/a n/a n/a n/a n/a n/a n/a n/a	These pins are reserved for future use, and should not be connected.
Note: *STANDBY#, RCLK, GPIO0, and GPIO1 are powered by DVCC and GND.*				

2.5 M38813

2.5.1 Overview

The M38813M4-XXXHP is an 8-bit single-chip microcomputer created in a silicon gate CMOS process. Built into this single-chip microcomputer are:

- Serial I/O function (either clock synchronous or UART method selectable in software)
- 8-bit timers
- 8-bit Comparator
- Double Bus interface

The M38813M4-XXXHP is designed as a dedicated microcomputer for Keyboard controller. The reduced power dissipation of the CMOS process also makes this microcomputer extremely useful for applications utilizing battery power.

2.5.2 Description

The functions of the M38813M4-XXXHP are outlined in Table1.1.1. In this manual, the suffix HP indicates a 0.5mm-lead pitch QFP.

Table 2-9 M38813M4-XXXHP Functions

Parameter	Function	
Basic instructions	71	
Instruction execution time	0.5μs (shortest instruction, at 8MHz oscillation frequency)	
Oscillation frequency	8MHz (max.)	
Memory size	ROM	16384 bytes of user area
	RAM	512 bytes
Input/output ports	P0-P4	8-bit X 5
	P5	4-bit X 1
	P6	2-bit X 1
Serial I/O	Clock synchronous or asynchronous	
Timers	8-bit prescaler x 2 and 8-bit timer x 3	
Comparator	4-bit resolution x 8 channels	
Bus interface	Two 8-bit Master CPU bus interface	
Key on wake up	8 inputs	
Interrupts	8 external, 9 internal, 1 software	
Clock generation circuit	Built-in (connect to external ceramic resonator or quartz crystal oscillator)	
Supply voltage	$f(X_{IN})$=8MHz	4.0 to 5.5V
	$f(X_{IN})$=4MHz	2.7 to 5.5V
Power dissipation	40mW (at 8MHz oscillation frequency, typ.)	
Input/output characteristics	Input/output break-down voltage	5V

Table 2-9 M38813M4-XXXHP Functions

Parameter	Function	
	Output current	10mA (15mA for $P2_4$-$P2_7$)
Operating temperature range	-20 to 85°C	
Device structure	CMOS silicon gate	
Package	M38813M4-XXXHP	64-pin plastic molded QFP (0.5mm-lead pitch)

2.5.3 Pin Configuration

The Pin configuration of the M38813M4-XXXHP is shown in below.

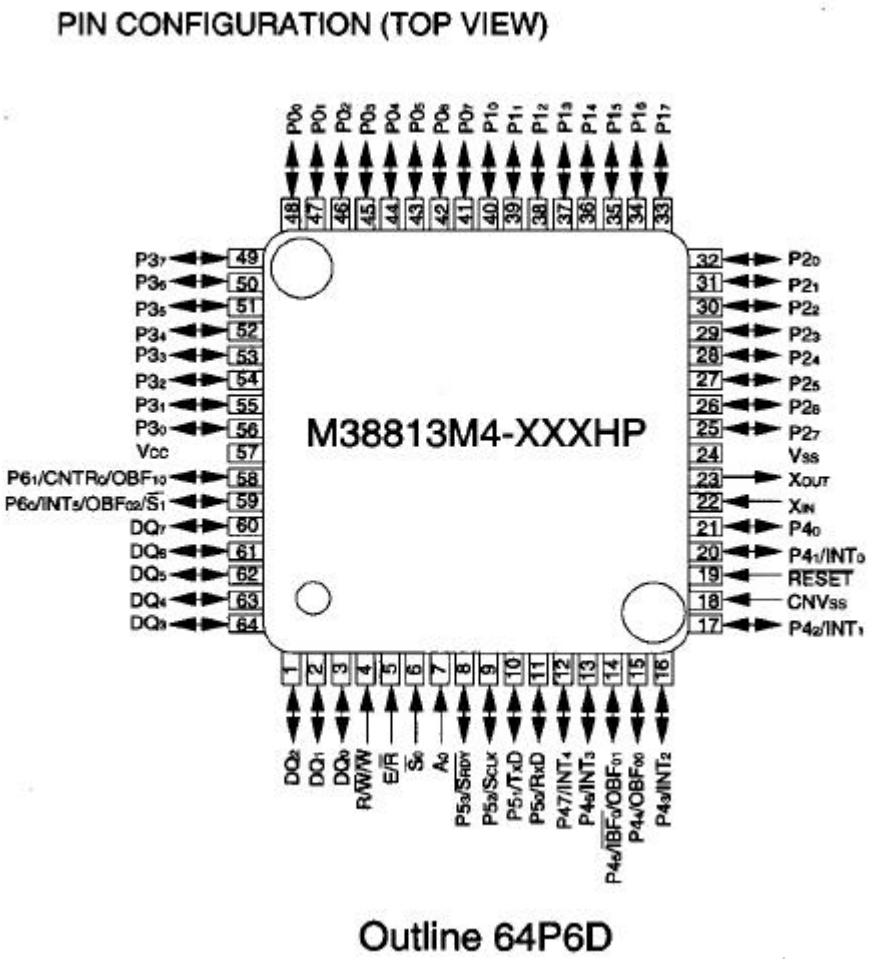


Figure 2-9 M38813 Pin Diagram

2.5.4 Pin Descriptions

The pin functions are listed in the table below.

Table 2-10 M38813M4-XXXHP Pin Description

Pin	Name	Function
Vcc, Vss	Power supply	Power supply inputs 2.7 to 5.5V to Vcc, and 0V to Vss.
CNVss	CNVss	Controls the operating mode of the chip. Normally connected to Vss or Vcc.
RESET	Reset input	To enter the reset state, this pin must be kept "L" for more than 2µs (under normal Vcc conditions). If the crystal or ceramic resonator requires more time to stabilize, extend this "L" level time as appropriate.
.XIN XOUT	Clock input Clock output	Input and output signals to and from the internal clock generation circuit. Connect a ceramic resonator or quartz crystal between the X_{IN} and X_{OUT} pins to set the oscillation frequency. If an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open.
$P0_0$-$P0_7$	I/O port P0	An 8-bit CMOS I/O port. An I/O direction register allows each pin to be individually programmed as either input or output. The input is CMOS/TTL level, and output is CMOS 3 state / Nch open drain
$P1_0$-$P1_7$	I/O port P1	An 8-bit CMOS I/O port with the same function as port P0. The input is CMOS/TTL level, and output is CMOS 3 state
$P2_O$-$P2_7$	I/O port P2	An 8-bit CMOS I/O port with the same function as port P0. The input is CMOS/TTL level, and output is CMOS 3 state. P_{24}-P_{27} is the LED driver port which capable of handling large current drive.
P3c-P37	I/O port P3	An 8-bit CMOS I/O port with the same functions as port P0. The input is CMOS level, and output is CMOS 3 state. This port is used as input of key on wake up and comparator functions. Pull-up transistor can be controlled by the program.
P40-P47	I/O port P4	An 8-bit I/O port with the same functions as port P0. The input is CMOS TTL level, and output of $P4_0$-$P4_3$,$P4_6$,$P4_7$ is Nch open drain. And The $P4_4$ and $P4_5$ are also used as the control signal outputs to the master CPU by selecting by the program.
P5c-P53	I/O port P5 ,	An 4-bit CMOS I/O port with the same functions as port P0. The input is CMOS level, and output is CMOS 3 state. The P5 also act as serial I/O function pins by selecting by the program.
P60-P61	I/O port P6	An 2-bit CMOS I/O port with the same functions as port P0. The input is CMOS level, and output is CMOS 3 state. The $P6_0$ also act as the control signal to the master CPU, and $P6_1$, act as I/O pin of the Timer X by selecting by the program.
Ao,So,E/R W / R/W	Input port	The control bus which control the interface between master CPU. The input is CMOS/TTL level, and output is CMOS 3 state.
DQo-DQ_7	Input port	An 8-bit Input port used to interface with the master CPU. The input TTL level, and output is CMOS/TTL level, and output is CMOS 3 state.

2.5.4.1 Functional Block Diagram

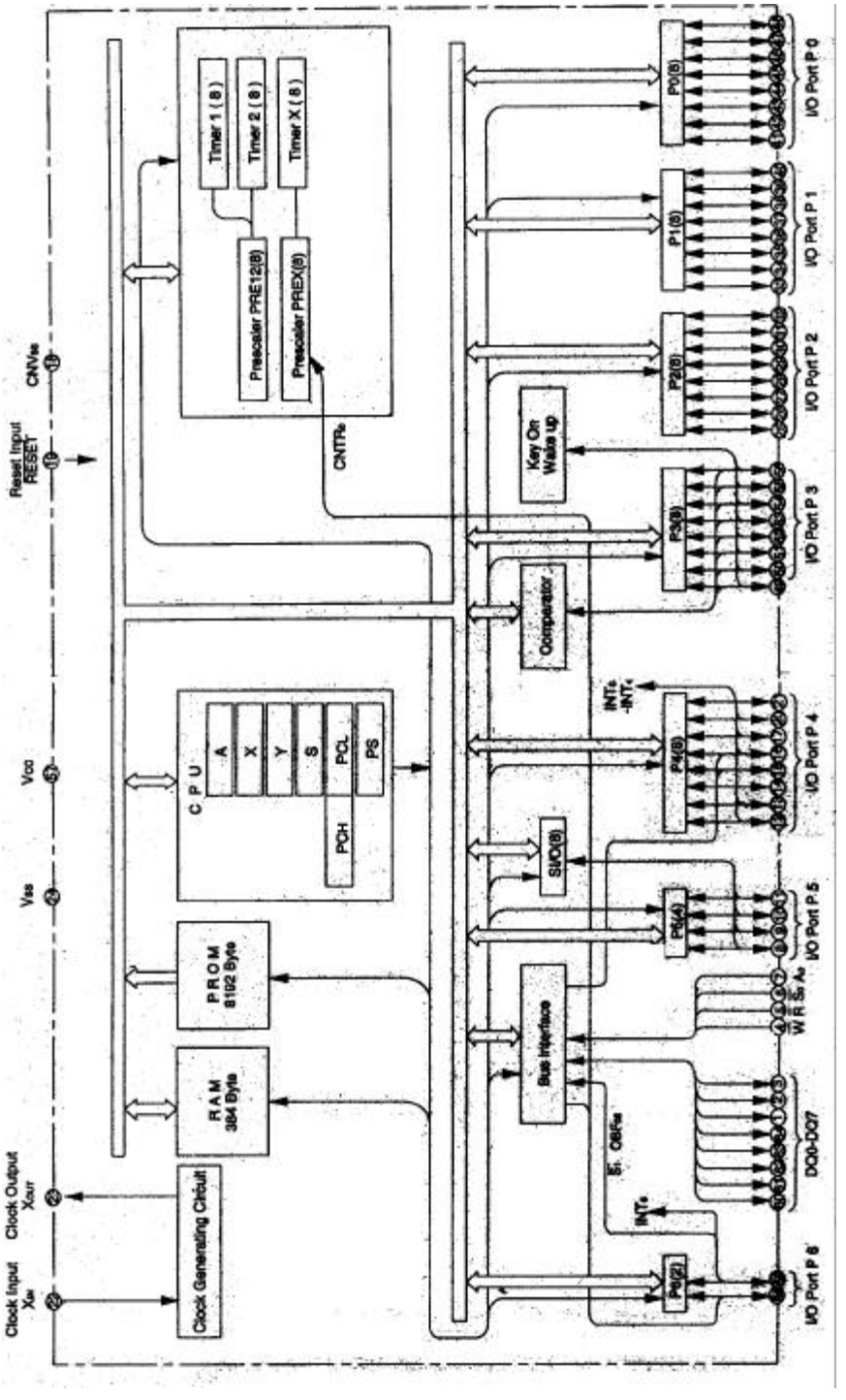


Figure 2-10 M38813 Block Diagram

2.6 YMF715B-S

YMF715-S (OPL3-SA3) is a single audio chip that integrates OPL3 and its DAC, 16 bit Sigma-delta CODEC, MPU401 MIDI interface, joystick with timer, and a 3D enhanced controller including all the analog components which is suitable for multi-media application. This LSI is fully compliant with Plug and Play ISA 1.0a, and supports all the necessary features, i.e. 16 bit address decode, more IRQs and DMAs in compliance with PC'96. This LSI also supports the expandability, i.e. Zoomed Video, Modem and CD-ROM interface in a Plug and Play manner, and power management (power down, power save, partial power down, and suspend/resume) that is indispensable with power-conscious application.

2.6.1 Features

- Built-in OPL3
- Supports Sound Blaster Game compatibility
- Supports Windows Sound System compatibility
- Supports Plug & Play ISA 1.0a compatibility
- Full Duplex operation
- Built-in MPU401 Compatible MIDI I/O port
- Built-in Joystick
- Built-in the 3D enhanced controller including all the analog components
- Supports multi-purpose pin function (Support 16-bit address decode, DAC interface for OPL4-ML, Zoomed Video port, EEPROM interface, MODEM interface, IDE CD-ROM interface)
- Hardware and software master volume control
- Supports monaural input
- 24 mA 1TL bus drive capability
- Supports Power Management(power down, power save, partial power down, and suspend/resume) ..
- +5V/ +3.3V power supply for digital, 5V power supply for analog.
- 100 pin SQFP package (YMF715-S)

2.6.2 Pin Diagram

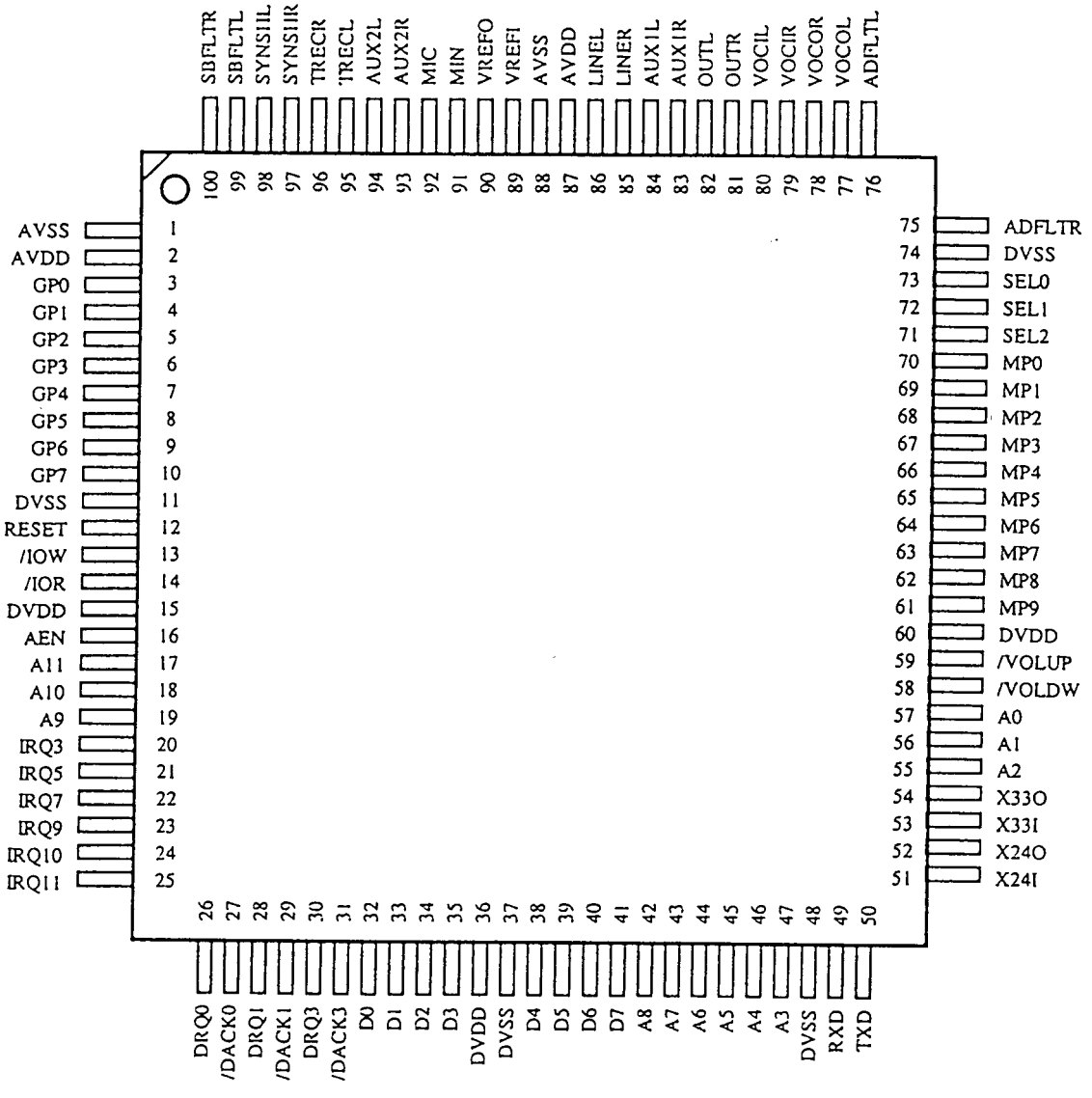


Figure 2-11 YMF715 Block Diagram

2.6.3 Pin Descriptions

Table 2-11 YMF715 Descriptions

Pin name	Pins	I/O	Type	Size	Function
ISA bus interface: 36 pins					
D7-0	8	I/O	TTL	24mA	Data Bus
AI 1-0	12	I	TTL	2mA	Address Bus
AEN	1	I	TTL	2mA	Address Bus Enable
/IOW	1	I	Schmitt	4mA	Write Enable
/IOR	1	I	Schmitt	4mA	Read Enable
RESET	1	I	Schmitt	4mA	Reset
IRQ3,5,7,9,10,11	6	T	TTL	12mA	Interrupt request
DRQ0,1,3	3	T	TTL	12mA	DMA Request
/DACK0, 1,3	3	I	TTL	2mA	DMA Acknowledge
Analog Input & Output : 24 sins					
OUTL	1	O	-	-	Left mixed analog output
OUTR	1	O	-	-	Right mixed analog output
VREFI	1	I	-	-	Voltage reference input
VREFO	1	O	-	-	Voltage reference output
AUXIL	I	I	-	-	Left AUX1 input
AUX1R	I	I	-	-	Right AUX1 input
AIJX2L	I	I	-	-	Left AUX2 input
AUX2R	1	I	-	-	Right AUX2 input
LINEL	1	I	-	-	Left LINE input
LINER	1	I	-	-	Right LINE input
MIC	1	I	-	-	MIC input
MIN	1	I	-	-	Monaural input
TRECL	1	-	-	-	Left Treble capacitor
TRECR	1	-	-	-	Right Treble-capacitor
SBFLTL	1	-	-	-	Left SBDAC filter
SBFLTR	1	-	-	-	Right SBDAC filter
SYNSHL	1	-	-	-	Left SYNDAC sample / hold capacitor
SYNSHR	1	-	-	-	Right SYNDAC sample / hold capacitor
ADFLTL	1	-	-	-	Left input filter
ADFLTR	1	-	-	-	Right input filter
VOCOL	1	O	-	-	Left voice output
VOCOR	I	O	-	-	Right voice output
VOCIL	1	I	-	-	Left voice input
VOCIR	1	I	-	-	Right voice input
Multi-purpose Dins: 13 pins					
SEL2-0	3	I+	CMOS	2mA	Refer to “Multi-purpose pins” section

Table 2-11 YMF715 Descriptions

Pin name	Pins	I/O	Type	Size	Function
MP9-0	l0	I+/O	TTL	4mA	Refer to “multi-purpose pins” section
Others: 27 pins					
GPO - GP3	4	IA	-	-	Game Port
GP4- GP7	4	I+	Schmitt	2mA	Game Port
RXD	1	I+	Schmitt	2rnA	MIDI Data Receive
TXD	1	O	TTL	4mA	MIDI Data Transfer
/VOLUP	1	I+	Schmitt	2mA	Hardware Volume (Up)
/VOLDW	l	I+	Schmitt	2mA	Hardware Volume (Down)
X331	1	I	CMOS	2mA	33.8688 MHz
X33O	1	O	CMOS	2mA	33.8688 MHz
X24I	1	I	CMOS	2mA	24.576 MHz
X24O	1	O	CMOS	2mA	24.576 MHz
AVDD	2	-	-	-	Analog Power Supply (put on +5.0V)
DVDD	3	-	-	-	Digital Power Supply (put on +5.0 V or +3.3V)
AVSS	2	-	-	-	Analog GND
DVSS	4	-	-	-	Digital GND

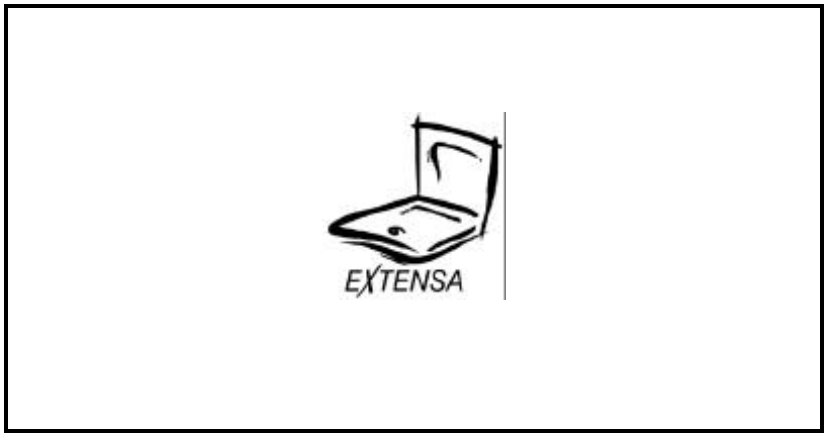
Note: *I+: Input Pin with Pull up Resistor*
Schmitt: TTL-Schmitt input pin
T: TTL-tri-state output pin
O+: Output Pin with Pull up Resistor

BIOS Setup Information

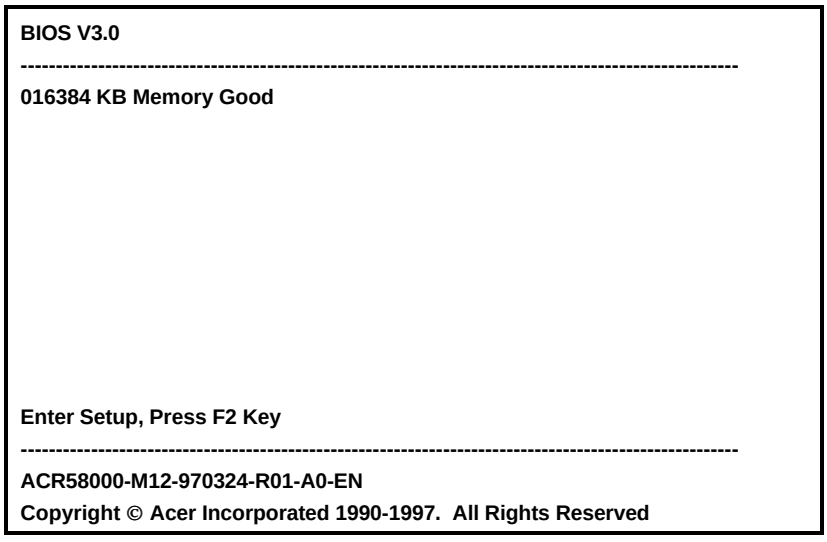
The Setup Utility is a hardware configuration program built into your computer's BIOS (Basic Input/Ouput System).

Your computer is already properly configured and optimized, and you do not need to run this utility. However, if you encounter configuration problems, you may need to run Setup. Please also refer to Appendix E, BIOS Post Checkpoints when a problem arises.

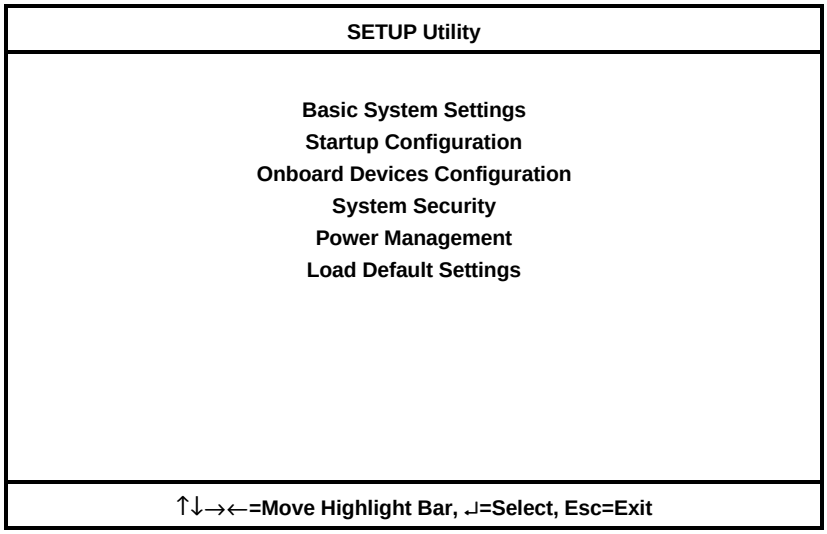
To activate the Setup Utility, press **F2** after you hear a beep while the Extensa logo is being displayed.



When Silent Boot (described later in this chapter) is disabled, a message displays telling you when you can press F2 to run the Setup Utility.



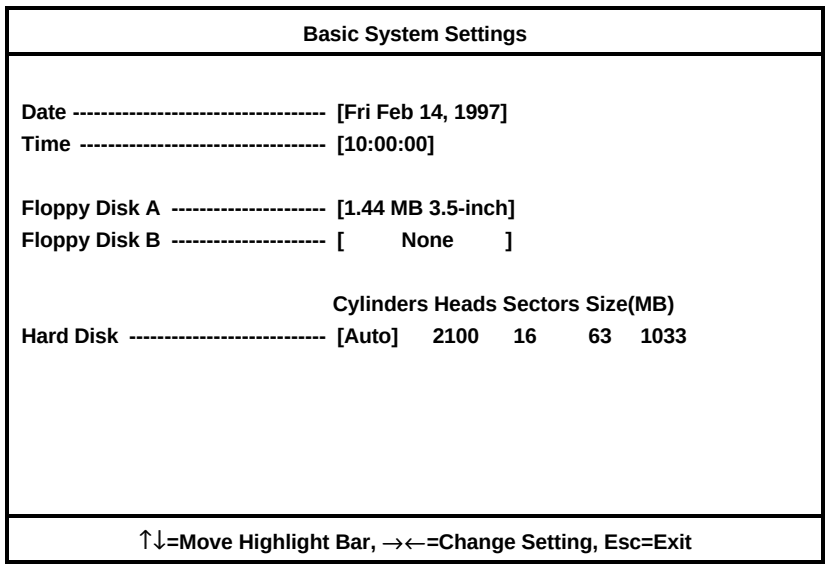
Pressing **F2** brings up the main screen of the Setup Utility.



Press the cursor keys (↑↓→←) to move the highlight bar, then press **Enter** to make a menu selection.

3.1 Basic System Settings

The Basic System Settings screen contains parameter items involving basic computer settings.



Press ↑ and ↓ to move the highlight bar; press → and ← to change the setting of the highlighted parameter. To exit this screen and return to the main screen, press **Esc**.

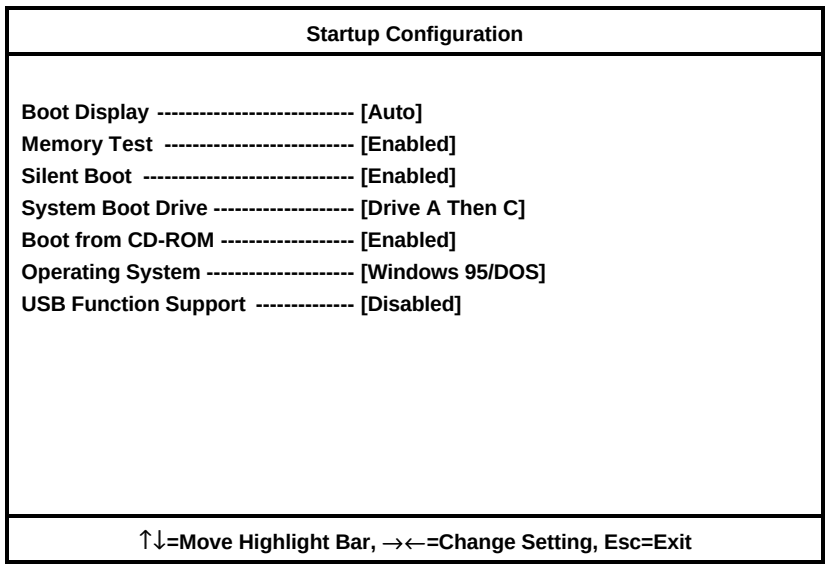
The following table describes the parameters in this screen. Settings in **boldface** are the default and suggested parameter settings.

Table 3-1 Basic System Settings Parameters

Parameter	Description	Setting or Format
Date	Sets the computer's system date	Day of the Week-Month-Day-Year
Time	Sets the computer's system time	Hour:Min:Sec
Floppy Disk A	Selects the floppy disk drive type.	**1.44 MB 3.5-inch** None
Floppy Disk B	Selects the floppy disk drive type. In most cases, you only have need for one floppy disk drive (A), so this is normally set to None.	**None** 1.44 MB 3.5-inch
Hard Disk	Selects the hard disk drive type. When set to User, you need to specify the Cylinder, Head and Sector information. For hassle-free and correct drive detection, this should be set to Auto.	**Auto** User None

3.2 Startup Configuration

The Startup Configuration screen contains parameter items that are set-up when the computer starts up.



Press ↑ and ↓ to move the highlight bar; press → and ← to change the setting of the highlighted parameter. To exit this screen and return to the main screen, press **Esc**.

The following table describes the parameters in this screen. Settings in **boldface** are the default and suggested parameter settings.

Table 3-2 Startup Configuration Parameters

Parameter	Description	Setting
Boot Display	Sets the display device (computer LCD and/or external monitor) to use when the computer starts (boots) up. When set to Auto, the computer outputs to the external monitor if one is connected; otherwise, the computer outputs to the LCD.	**Auto** Both
Memory Test	Runs or skips the memory test.	**Enabled** Disabled
Silent Boot	Hides or displays or hides the POST (Power On Self Test) screen messages.	**Enabled** Disabled
System Boot Drive	Sets the startup (boot) sequence of the drives in your computer. For example, when set to Drive A Then C, the computer searches for a system (bootable) diskette in drive A first before proceeding with drive C.	**Drive A Then C** Drive C Then A Drive C Drive A
Boot from CD-ROM	Tells the computer to search for a bootable disc in the CD-ROM drive and boot from that disc. If the computer cannot find a bootable disc, it proceeds according to the System Boot Drive parameter setting.	**Enabled** Disabled

Table 3-2 Startup Configuration Parameters

Parameter	Description	Setting
Operating System	Selects the operating system the computer is running. Set this parameter to the appropriate OS to get maximum performance.	**Windows 95/DOS** Windows NT
USB Function Support	Selects support for USB (Universal Serial Bus). Enable this parameter if you are connecting USB device(s) to the computer.	**Disabled** Enabled

3.3 Onboard Devices Configuration

The Onboard Devices Configuration screen contains parameter items that are related to port devices on your computer.

Onboard Devices Configuration	
Serial Port	**[Enabled]**
Base Address	**[3F8h]**
IRQ	**[4]**
IrDA FIR	**[Enabled]**
Base Address	**[2F8h]**
IRQ	**[3]**
DMA	**[3]**
Internal Modem	**[Enabled]**
Base Address	**[3E8h]**
IRQ	**[11]**
Parallel Port	**[Enabled]**
Base Address	**[378h]**
IRQ	**[7]**
Operation Mode	**[Bi-directional]**
ECP DMA Channel	[-]
↑↓=Move Highlight Bar, →←=Change Setting, Esc=Exit	

Press ↑ and ↓ to move the highlight bar; press → and ← to change the setting of the highlighted parameter. To exit this screen and return to the main screen, press **Esc**.

The following table describes the parameters in this screen. Settings in **boldface** are the default and suggested parameter settings.

Table 3-3 Onboard Devices Configuration Parameters

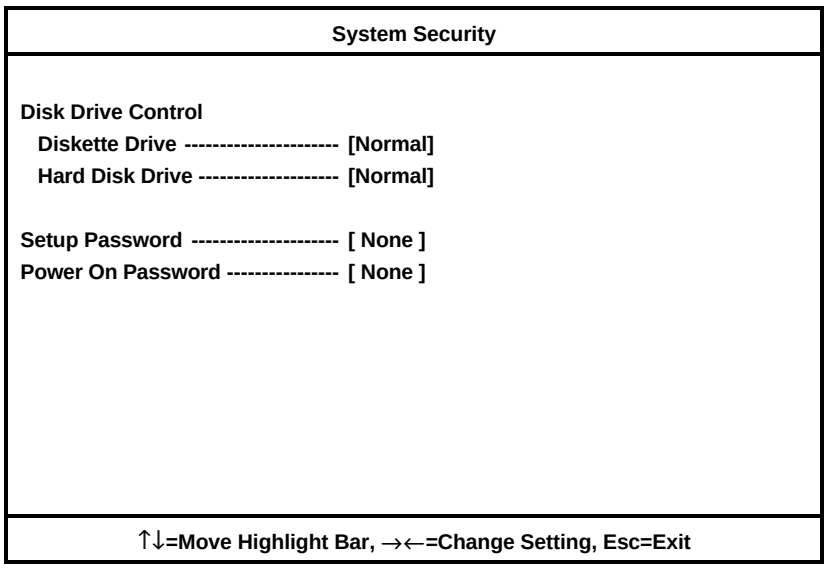
Parameter	Description	Setting
Serial Port	Enables or disables the serial port	**Enabled** Disabled
Base Address	Sets the I/O base address of the serial port	**3F8h** 2F8h 3E8h 2E8h
IRQ	Sets the IRQ (interrupt request) channel of the serial port	**4** 11
IrDA FIR	Enables or disables the infrared port	**Enabled** Disabled
Base Address	Sets the I/O base address of the infrared port	**2F8h** 3E8h 2E8h 3F8h
IRQ	Sets the IRQ channel of the infrared port	**3** 10

Table 3-3 Onboard Devices Configuration Parameters

Parameter	Description	Setting
DMA	Sets the DMA (direct memory access) channel of the infrared port	**3** 1
Internal Modem	Enables or disables the internal modem	**Enabled** Disabled
Base Address	Sets the I/O base address of the internal modem	**3E8h** 3F8h 2F8h 2E8h
IRQ	Sets the IRQ channel of the internal modem	**11** 5 3 4 10
Parallel Port	Enables or disables the parallel port	**Enabled** Disabled
Base Address	Sets the I/O base address of the parallel port	**378h** 278h 3BCh
IRQ	Sets the interrupt request (IRQ) channel of the parallel port	**7** 5
Operation Mode	Selects the operation mode of the parallel port. ECP (Extended Capabilities Port) supports a 16-byte FIFO (first in, first out) which can be accessed by host DMA cycles and PIO cycles, boosting I/O bandwidth to meet the demands of high-performance peripherals.	**Bi-directional** ECP Standard
ECP DMA Channel	Sets the DMA channel of the parallel port when the parallel operation mode is set to ECP.	**1** 3

3.4 System Security

The System Security screen contains parameter items that help safeguard and protect your computer from unauthorized use.



Press ↑ and ↓ to move the highlight bar; press → and ← to change the setting of the highlighted parameter. To exit this screen and return to the main screen, press **Esc**.

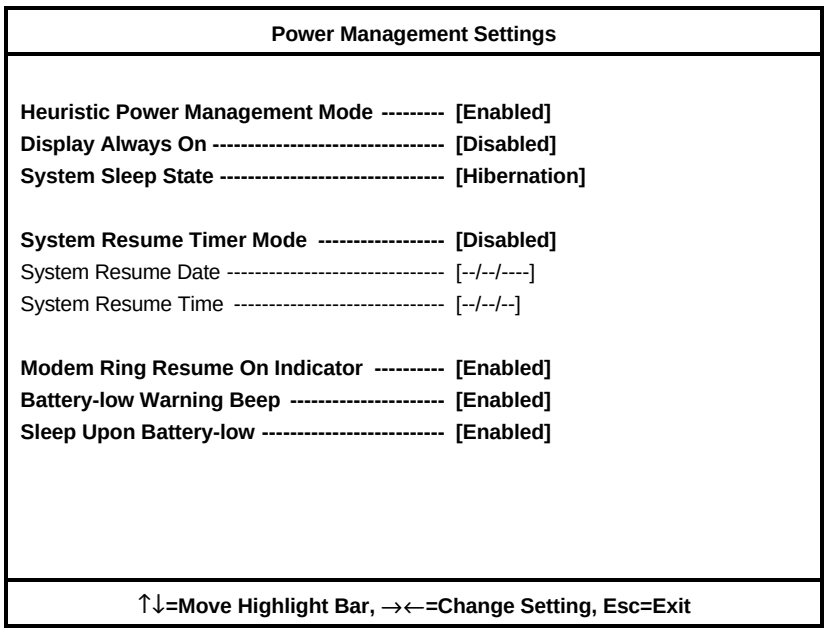
The following table describes the parameters in this screen. Settings in **boldface** are the default and suggested parameter settings.

Table 3-4 System Security Parameters

Parameter	Description	Setting
Diskette Drive (Control)	Sets the control level of the diskette drive.	**Normal** Disabled Write Protect All Sectors Write Protect Boot Sector
Hard Disk Drive (Control)	Sets the control level of the diskette drive.	**Normal** Disabled Write Protect All Sectors Write Protect Boot Sector
Setup Password	Sets (and enables) the setup password. When set, this password protects this Setup Utility from unauthorized entry. Before the computer allows access to the Setup Utility, you need to enter the setup password.	**None** Enabled
Power On Password	Sets (and enables) the power on password. When set, this password protects the computer from unauthorized entry. At startup, you need to enter the power on password to continue computer operation.	**None** Enabled

3.5 Power Management Settings

The Power Management Settings screen contains parameter items related to power-saving and power management.



Press ↑ and ↓ to move the highlight bar; press → and ← to change the setting of the highlighted parameter. To exit this screen and return to the main screen, press **Esc**.

The following table describes the parameters in this screen. Settings in **boldface** are the default and suggested parameter settings.

Table 3-5 Power Management Settings Parameters

Parameter	Description	Setting or Format
Heuristic Power Management Mode	Enables or disables heuristic power management mode.	**Enabled** Disabled
Display Always On	When enabled the computer does not enter display standby mode.	**Disabled** Enabled
System Sleep State	Setting this item determines which power management mode (Hibernation or Standby) the computer enters into when you press the Sleep hotkey (Fn-F7).	**Hibernation** Standby
System Resume Timer Mode	When enabled and the system resume date and time are valid, the computer resumes (wakes up) at the set time and date.	**Disabled** Enabled
System Resume Date	Sets the date the computer resumes (wakes up) from if the system resume timer is enabled.	month/day/ year
System Resume Time	Sets the time the computer resumes (wakes up) from if the system resume timer is enabled.	hour/minute/second

Table 3-5 Power Management Settings Parameters

Parameter	Description	Setting or Format
Modem Ring Resume On Indicator	When enabled, and an incoming modem ring is detected, the computer wakes up from standby mode. When the computer is off or in hibernation mode, the computer will not resume on a modem ring.	**Enabled** Disabled
Battery-low Warning Beep	Enables or disables warning beeps during a battery-low condition.	**Enabled** Disabled
Sleep Upon Battery-low	Enables or disables the sleep function (hibernation or standby) during a battery-low condition. When the computer is running very low on battery power, the computer will disregard the system sleep state setting and enter hibernation mode if Sleep Manager is installed and the hibernation file is valid.	**Enabled** Disabled

Pressing **Fn-F6** during normal computer operation (after POST) also brings up the power management screen. An additional page, shown below, is added to this function which appears only via **Fn-F6**.

System Information Reference

Serial Number	**: 11111111117**		
System BIOS Version	**: V3.0 R01-A0-EN**		
BIOS Release Date	**: 2/14/97**		
VGA BIOS Version	**: 0.2.5 R01-F0**		
Processor	**: Pentium**	**Internal Cache**	**: 16KB, Enabled**
Processor Speed	**: 150 MHz**	**External Cache**	**: 256KB, Enabled**
Total Memory	**: 16 MB**	**Pointing Device**	**: Detected**
Video Memory	**: 2 MB**	**Serial Port**	**: 3F8h, IRQ4**
Floppy Drive A	**: 1.44 MB**	**Irda FIR**	**: 2F8h, IRQ3, DMA3**
Floppy Drive B	**: None**	**Internal Modem**	**: 3E8h, IRQ11**
Hard Disk	**: 1033 MB**	**Parallel Port**	**: 378h, IRQ7**
CD ROM	**: Installed**	**Operation Mode**	**: Bi-directional**
CD ROM Bootable	**: Enabled**		
System Boot Drive	**: Drive A Then C**		

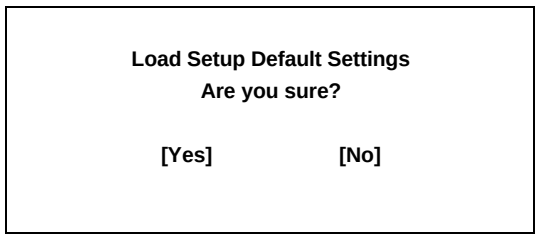
Esc=Exit

The System Information Reference screen gives a summary of your computer's BIOS information. These items are easy to understand and are self-explanatory.

Note: *The Serial Number and BIOS Versions are important information about your computer. If you experience computer problems, this data helps our service personnel know more about your computer.*

3.6 Load Default Settings

When you select the Load Default Settings item from the main screen, a dialog box appears asking you to confirm that you want to reset all settings to their factory defaults.



Choose **Yes** to confirm or **No** if otherwise.

Disassembly and Unit Replacement

This chapter contains step-by-step procedures on how to disassemble the notebook computer for maintenance and troubleshooting.

To disassemble the computer, you need the following tools:

- Wrist grounding strap and conductive mat for preventing electrostatic discharge
- Flat-bladed screwdriver
- Phillips screwdriver
- Hexagonal screwdriver
- Tweezers
- Plastic stick

The screws for the different components vary in size. During the disassembly process, group the screws with the corresponding components to avoid mismatch when putting back the components.

4.1 General Information

4.1.1 Before You Begin

Before proceeding with the disassembly procedure, make sure that you do the following:

1. Turn off the power to the system and all peripherals.
2. Unplug the AC adapter and all power and signal cables from the system.
3. Press the battery compartment cover release button and slide out the cover.
4. Pull out the battery pack using the pull loop at the end.

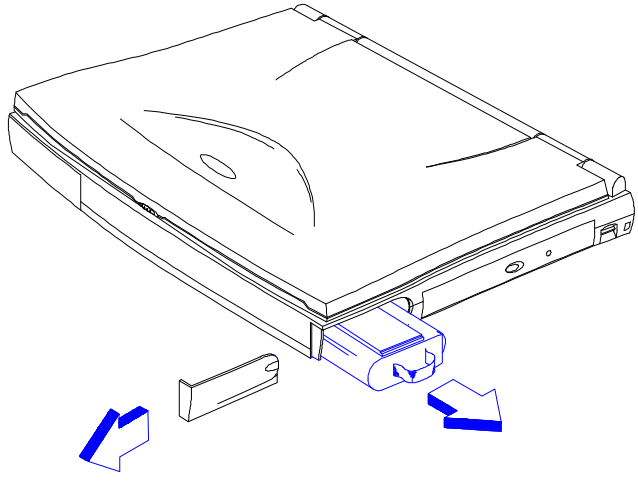


Figure 4-1 Removing the Battery Pack

Removing all power sources from the system prevents accidental short circuit during the disassembly process.

4.1.2 Connector Types

There are two kinds of connectors on the main board:

- Connectors with no locks

  Unplug the cable by simply pulling out the cable from the connector.

- Connectors with locks

  You can use a plastic stick to lock and unlock connectors with locks.

The cables used here are special FPC (flexible printed-circuit) cables, which are more delicate than normal plastic-enclosed cables. Therefore, to prevent damage, make sure that you unlock the connectors before pulling out the cables. Do not force cables out of the connectors.

CONNECTORS WITH LOCKS

- Unplugging the Cable

  To unplug the cable, first unlock the connector by pulling up the two clasps on both sides of the connector with a plastic stick. Then carefully pull out the cable from the connector.

- Plugging the Cable

  To plug the cable back, first make sure that the connector is unlocked, then plug the cable into the connector. With a plastic stick, press the two clasps on both sides of the connector to secure the cables in place.

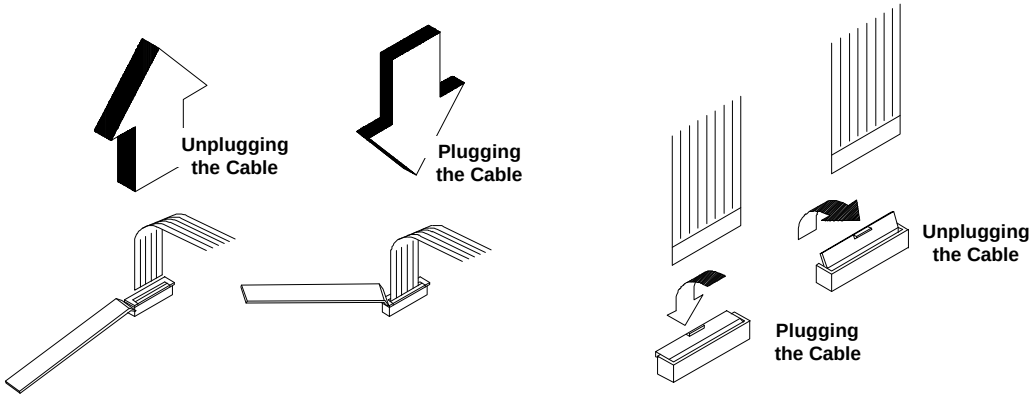


Figure 4-2 Using Connectors With Locks

Connectors mentioned in the following procedures are assumed to be no-lock connectors unless specified otherwise.

4.1.3 Disassembly Sequence

The disassembly procedure described in this manual is divided into four major sections:

- Section 4.2: Installing memory
- Section 4.3: Removing the modem board
- Section 4.4: Removing the hard disk drive
- Section 4.5: Removing the keyboard
- Section 4.6: Disassembling the inside frame assembly
- Section 4.7: Disassembling the display

The following table lists the components that need to be removed during servicing. For example, if you want to remove the motherboard, you must first remove the keyboard, then disassemble the inside assembly frame in that order.

Table 4-1 Guide to Disassembly Sequence

Service Item	Prerequisite
Remove or replace the hard disk drive	
Remove or replace the internal module	Remove the keyboard (and heat sink assembly).
Remove the motherboard for service or replacement	1. Remove the keyboard. 2. Disassemble the housing.
Remove the touchpad	1. Remove the keyboard. 2. Disassemble the housing.
Replace the LCD	Remove the display.
Install CPU	Remove the keyboard (and heat sink assembly).
Install additional memory	

The flowchart on the succeeding page gives a clearer and more graphic representation on the entire disassembly sequence. Please refer to it from time to time, together with the screw list below.

SCREW LIST

• A screw	M2x4L Black	(p/n: 86.1AI22.4R0)
• B screw	M2x6L NI	(p/n: 86.1A522.6R0)
• C screw	M2x20L NI	(p/n: 86.1A522.200)
• D screw	M2.5x8L NYLOK B-ZN	(p/n: 86.1A353.8R0)
• E screw	M2.5x6L NYLOK NI	(p/n:86.1A553.6R0)
• F screw	M3x6L BIND NI	(p/n:86.4A524.6R0)
• G screw	M2.5x4L C-ZN	(p/n: 86.1A423.4R0)
• H screw	M2x14L NI	(p/n: 86.1A522.140)
• I screw	M2x4L NI	(p/n: 86.1A522.4R0)
• J screw cap	M2*L5 NI	(p/n: 86.7A522.5R0)

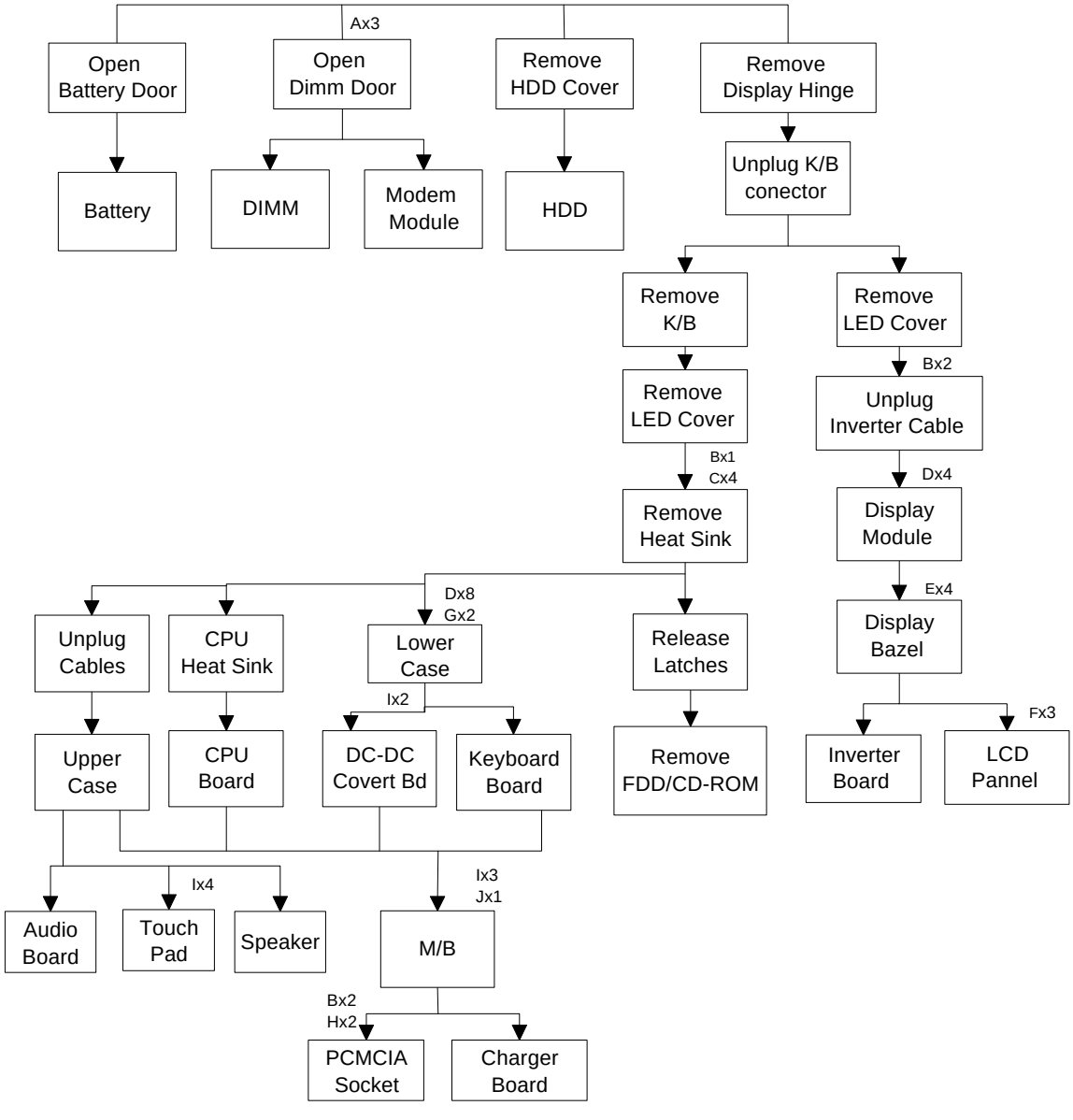


Figure 4-3 Disassembly Sequence Flowchart

4.2 Installing Memory

Follow these steps to insert memory modules:

1. Turn off the computer. Then turn the computer over to access its base.

2. Remove three screws from the memory door; then lift up and remove the memory door.

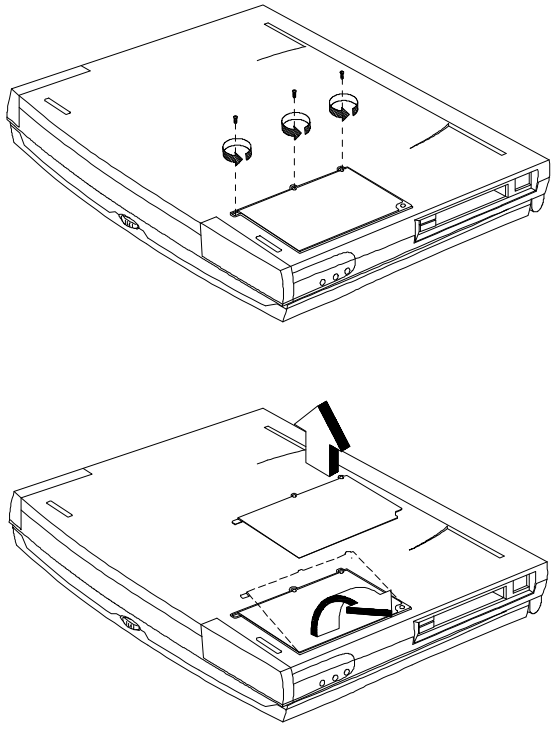


Figure 4-4 Removing the Memory Door

3. Remove the memory modules from its shipping container.

4. Align the connector edge of the memory module with the key in the connector. Insert the edge of the memory module board into the connector. Use a rocking motion to fully insert the module. Push downward on each side of the memory module until it snaps in place.

   To remove the memory module, release the slot locks found on both ends of the memory slot to release the DIMM. Then pull out the memory module.

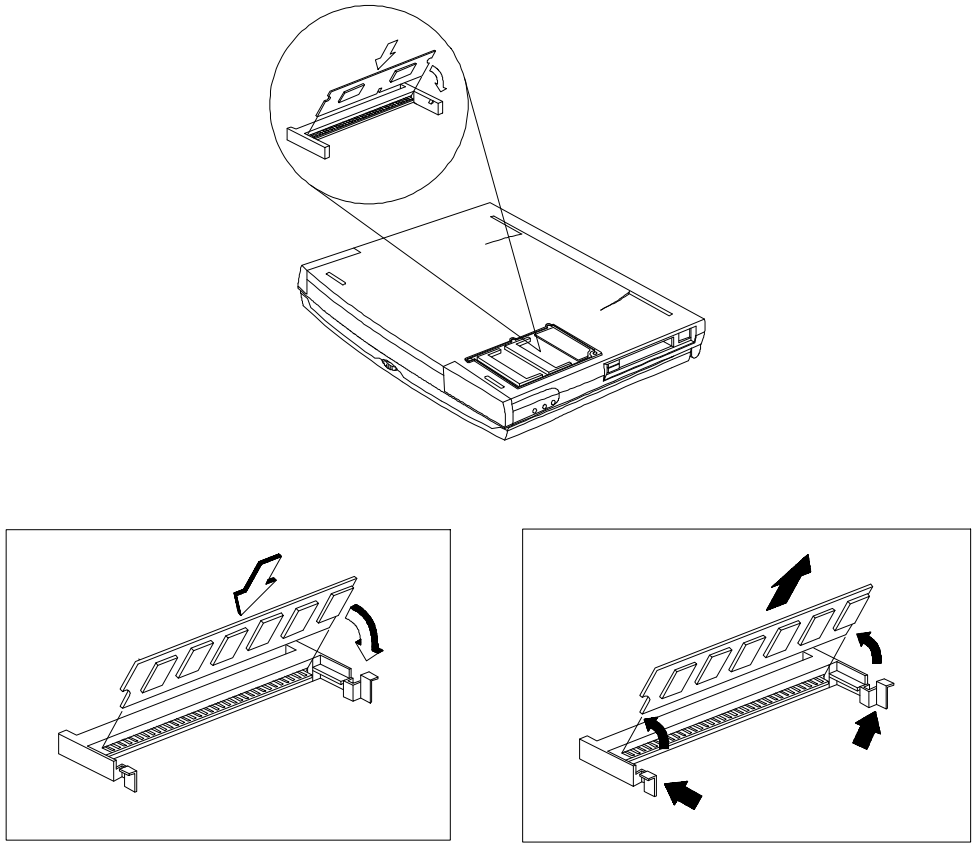


Figure 4-5 Installing and Removing Memory

5. Replace the memory door and secure it with the screws.

Sleep Manager must be run after installing additional memory for the computer to hibernate properly. If Sleep Manager is active, it will automatically adjust the hibernation file on your notebook.

If you are using an operating system other than Windows 95 or DOS, you may need to re-partition your hard disk drive to allow for the additional memory. Check with your system administrator.

4.3 Removing the Modem Board

When you open the memory door, you can also access and replace the modem board. See figure below.

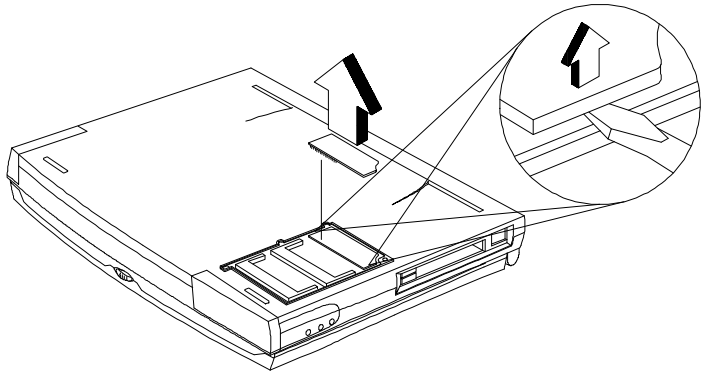


Figure 4-6 Removing the Modem Board

4.4 Removing the Hard Disk Drive

Follow these steps to remove the hard disk drive:

1. Turn the computer over and locate the hard disk drive bay cover.
2. Press the hard disk drive bay cover release and slide the cover out to remove it. Set aside the cover.
3. Pull the hard disk drive tab to remove the hard disk drive from the hard disk drive bay.

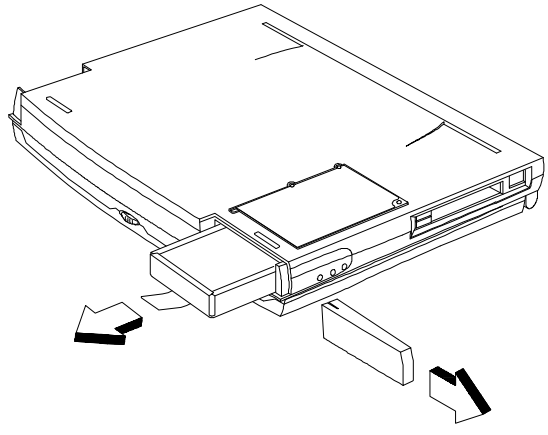


Figure 4-7 Removing the Hard Disk Drive

4. Store the hard disk drive in an antistatic bag.

If you want to install a new hard disk drive, reverse the steps described above.

4.5 Removing the Keyboard

Follow these steps to remove the keyboard:

1. Slide out the two display hinge covers on both sides of the notebook.

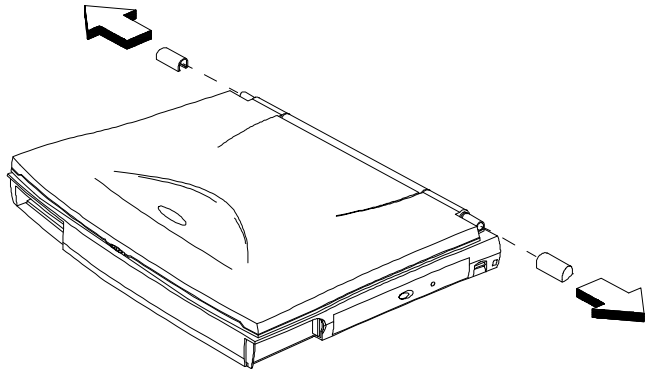


Figure 4-8 Removing the Display Hinge Covers

2. Using a pointed instrument, unlock the keyboard locks. Then pull out and flip down the keyboard to expose the keyboard connectors.

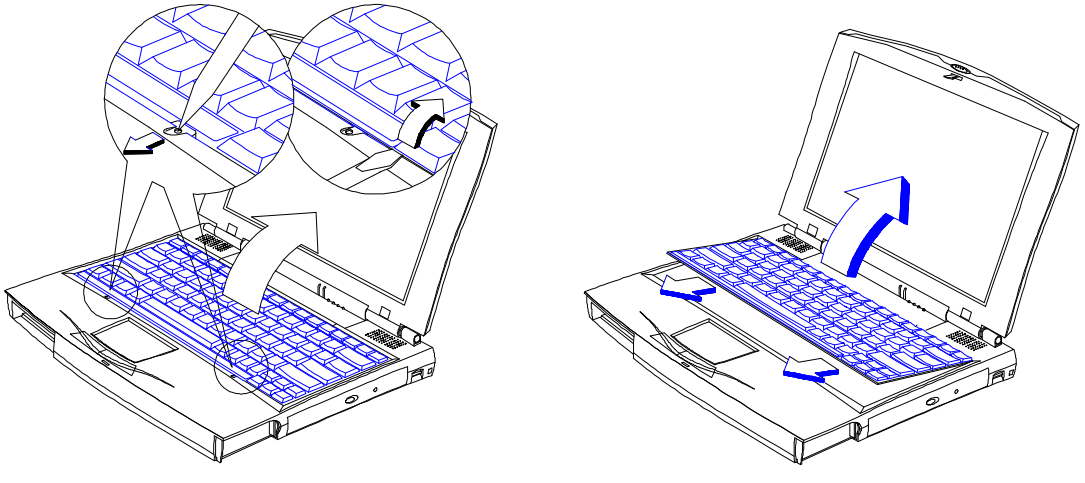


Figure 4-9 Removing the Keyboard

3. Unplug the keyboard connectors (CN3 and CN5) from the keyboard/touchpad board. Set aside the keyboard.

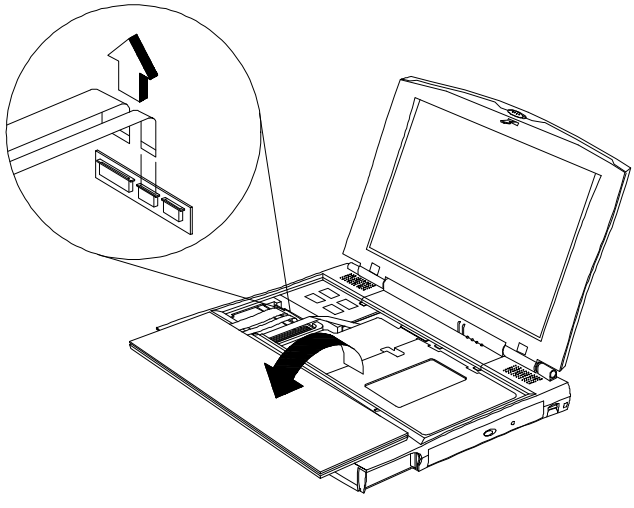


Figure 4-10 Unplugging the Keyboard Connectors

4.6 Disassembling the Inside Frame Assembly

This section discusses how to disassemble the housing, and during its course, includes removing and replacing of certain major components like the internal drive (CD-ROM or floppy), CPU and the main board. Follow these steps:

4.6.1 Removing the Heat Sink Assembly

Follow these steps to remove the heat sink assembly:

1. Pull up and remove the LED cover.

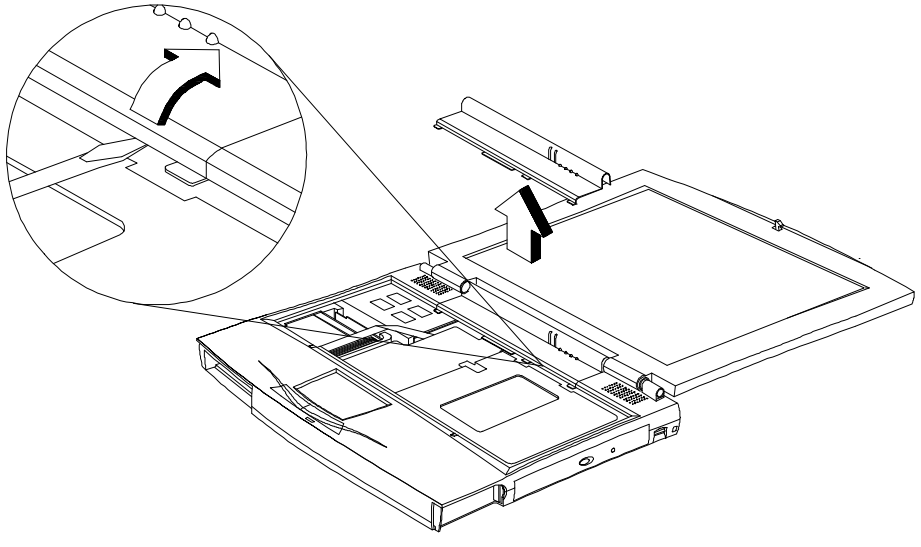


Figure 4-11 Removing the LED Cover

2. Remove the five screws that secure the heat sink assembly to the housing.

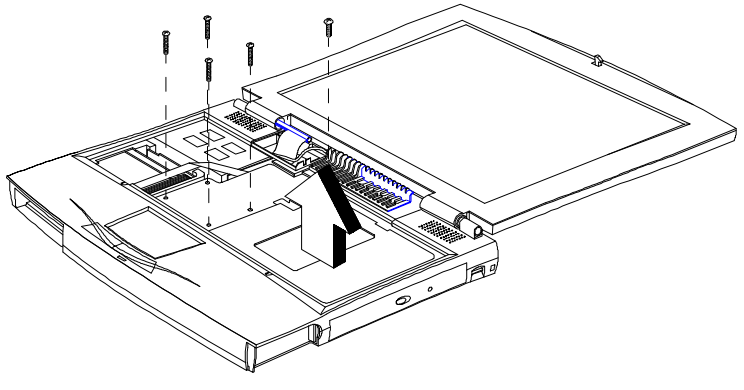


Figure 4-12 Removing the Heat Sink Assembly

4.6.2 Removing the Display

Follow these steps to remove the display:

1. Remove two screws on the bottom and two screws on the rear of the unit.

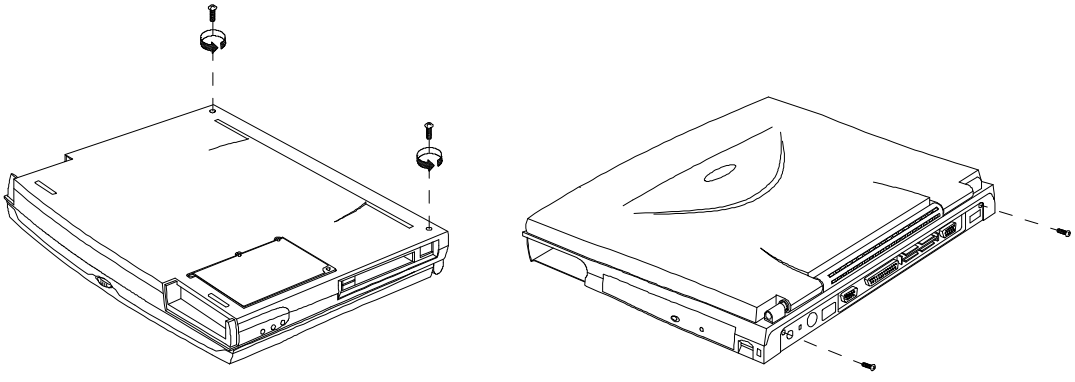


Figure 4-13 Unplugging the Display Cable

2. Open the display and remove two screws; then pull up the display cable (CN9) and unplug the inverter cable (CN8).

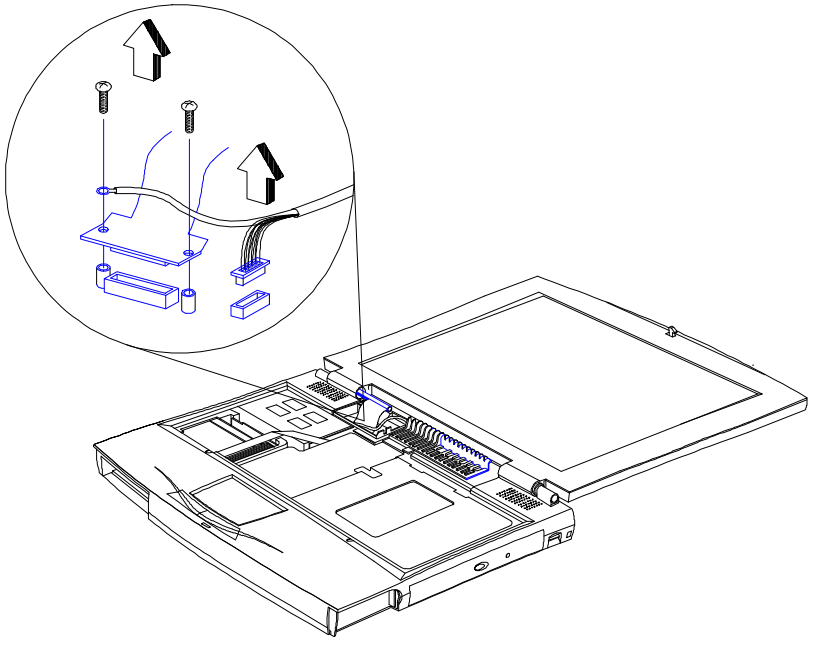


Figure 4-14 Removing the Display Hinge Screws

3. Detach the display from the main unit and set aside.

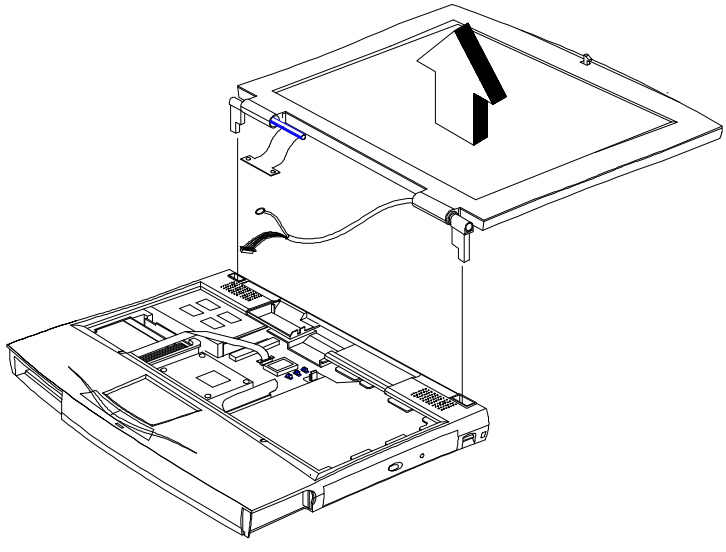


Figure 4-15 Removing the Display Hinge Screws

4.6.3 Removing the Internal Drive

Follow these steps to remove the internal drive:

1. Pull up the FDD/CD module latches.
2. Unplug the two internal drive cables (CN17 for FDD; CN17 and CN20 for CD-ROM).
3. Pull out the internal drive and set it aside.

Ensure the drive cables do not become hooked on the inside frame assembly when removing and reinstalling the drive.

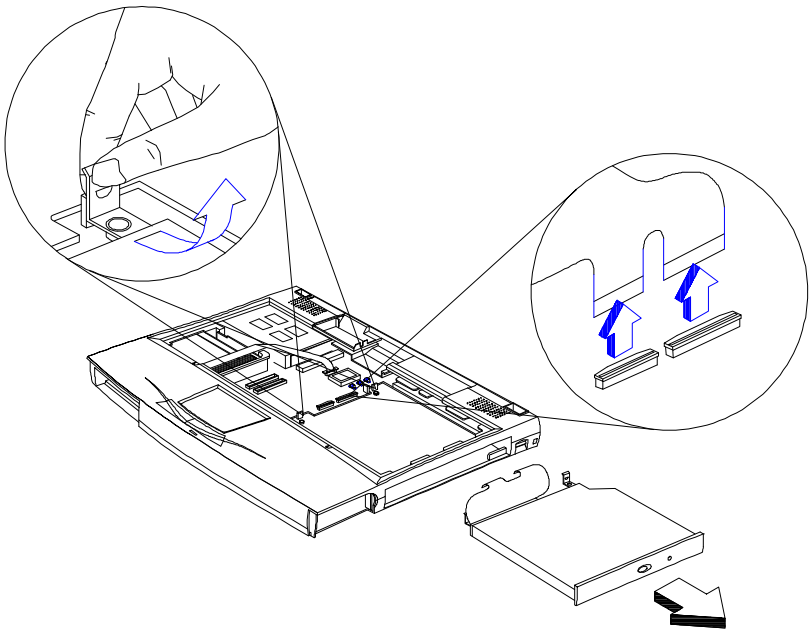


Figure 4-16 Removing the Internal Drive

4.6.4 Replacing the CPU

Gently pull out the CPU heat sink and the CPU board (CN21) from the mainboard.

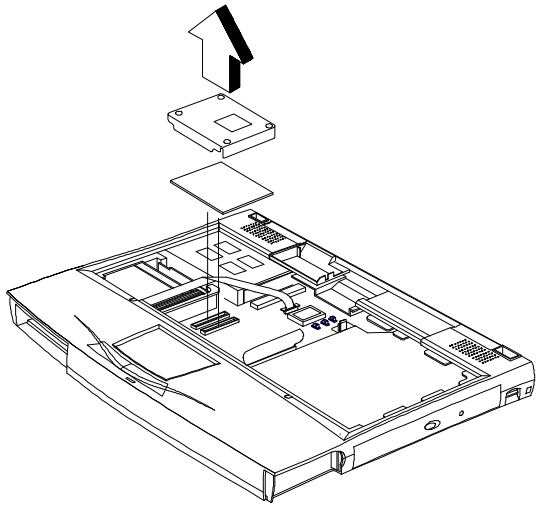


Figure 4-17 Replacing the CPU

Reverse the steps above to insert a replacement CPU.

4.6.5 Detaching the Top Cover

Follow these steps to detach the top cover from the bottom cover:

1. Unplug the touchpad cable (CN6) from the keyboard/touchpad board, and the audio board cable (CN14), speaker cables (CN13 and CN15) and optionally, the fan connector found just above the speaker cables (CN12) from the mainboard.

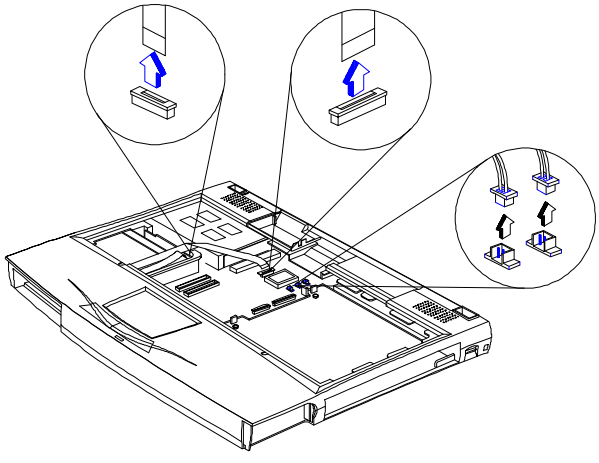


Figure 4-18 Removing Cables

2. Detach the top cover from the bottom cover.

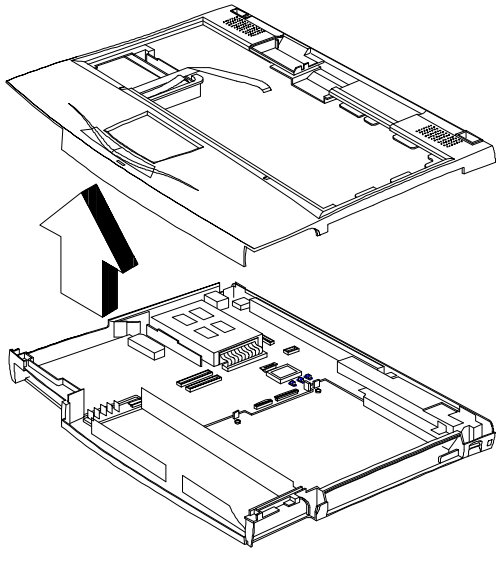


Figure 4-19 Detaching the Top Cover

4.6.6 Removing the Mainboard

Follow these steps to remove the mainboard:

1. Remove the screws found on the lower case (ten total screws, two screws shorter than the rest found on the front corners of the computer).

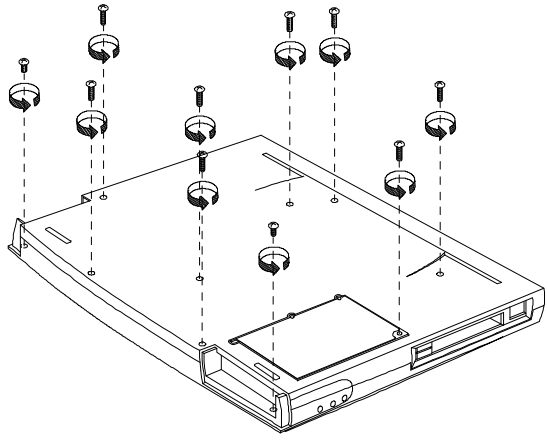


Figure 4-20 Removing the Bottom Screws

2. Remove the keyboard/touchpad board (CN18). Remove two screws and remove the plate that covers the DC-DC converter board.

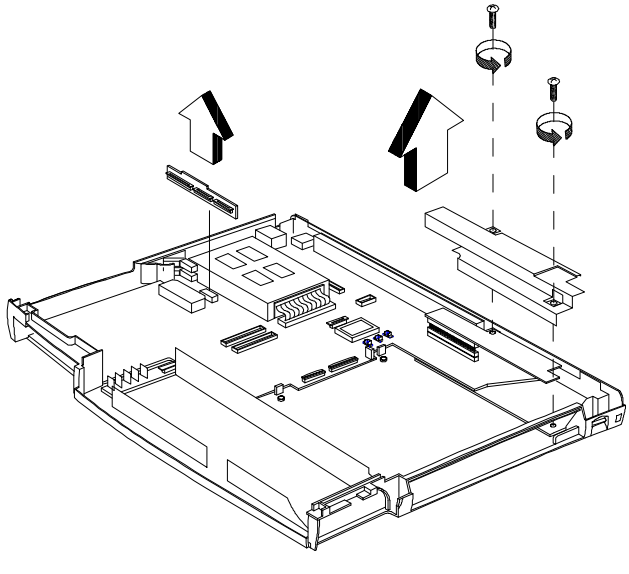


Figure 4-21 Removing the Keyboard/Touchpad Board and DC-DC Converter Board Cover

3. Gently remove the DC-DC converter board (CN7).

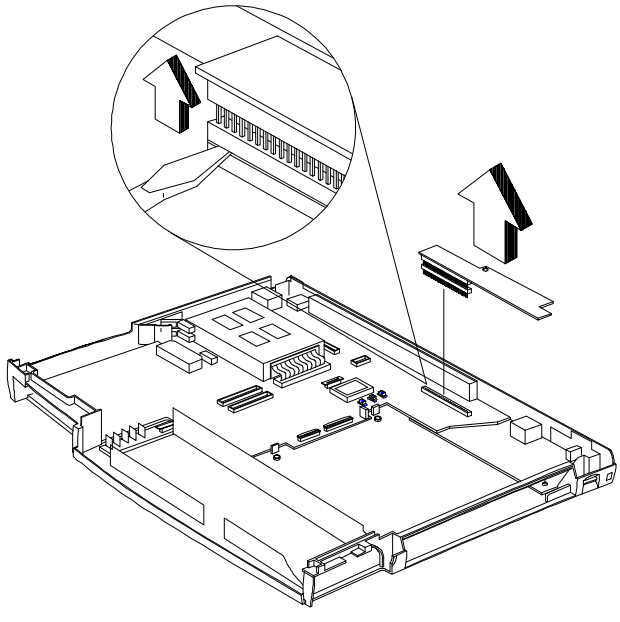


Figure 4-22 Removing the DC-DC Converter Board

4. Unplug the battery charger connector (CN22) and remove four screws that secure the motherboard to the base assembly. Then pull up to remove the mainboard.

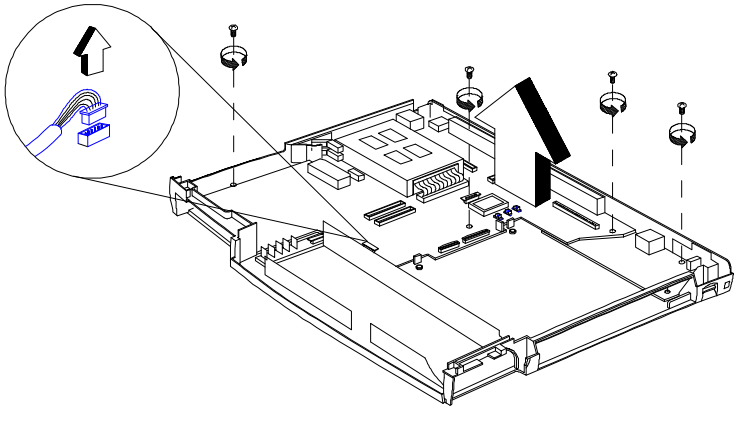


Figure 4-23 Removing the Mainboard

4.6.7 Disassembling the Mainboard

Follow these steps to disassemble the mainboard:

REMOVING THE CHARGER BOARD

Unplug the charger board (containing the power switch, DC-in jack and PS/2 port).

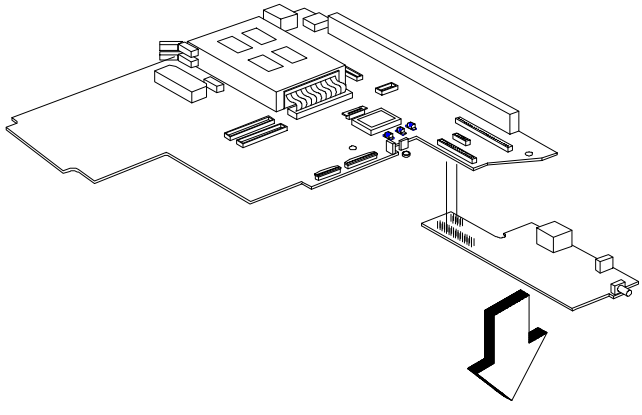


Figure 4-24 Removing the Charger Board

REMOVING THE PCMCIA SOCKETS

The PC Card Connector Module is normally part of the motherboard spare part. The following removal procedure is for reference only.

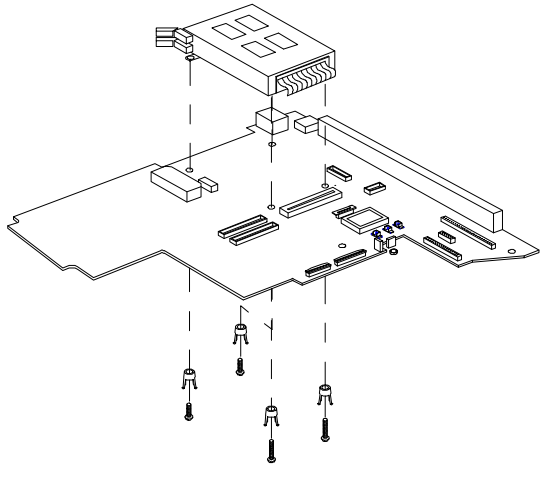


Figure 4-25 Removing the PCMCIA Sockets

4.6.8 Disassembling the Top Cover

The touchpad, speakers, audio board are connected to the top cover. The sections below describe the removal process of these components.

REMOVING THE HARD DISK DRIVE HEAT SINK

Pull up to remove the hard disk drive heat sink from the top cover.

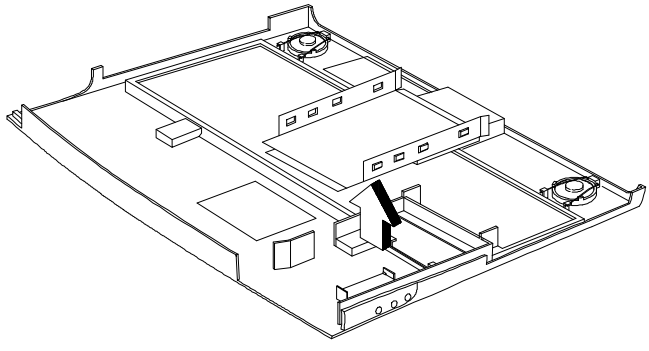


Figure 4-26 Removing the Hard Disk Drive Heat Sink

REMOVING THE AUDIO BOARD

Pull up to remove the audio board from the top cover.

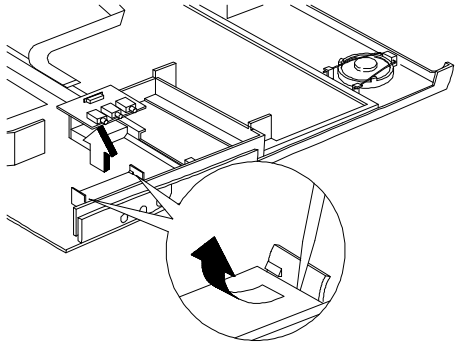


Figure 4-27 Removing the Audio Board

REMOVING THE TOUCHPAD

1. Remove four screws and lift up the metal plate and touchpad buttons.
2. Unplug the touchpad cable (J1) and remove the touchpad main sensor and connector unit.

REMOVING THE SPEAKERS

1. Unlock the speaker by pushing outward on its locks.
2. The flip up the wire that holds the speaker in place and remove the speaker.

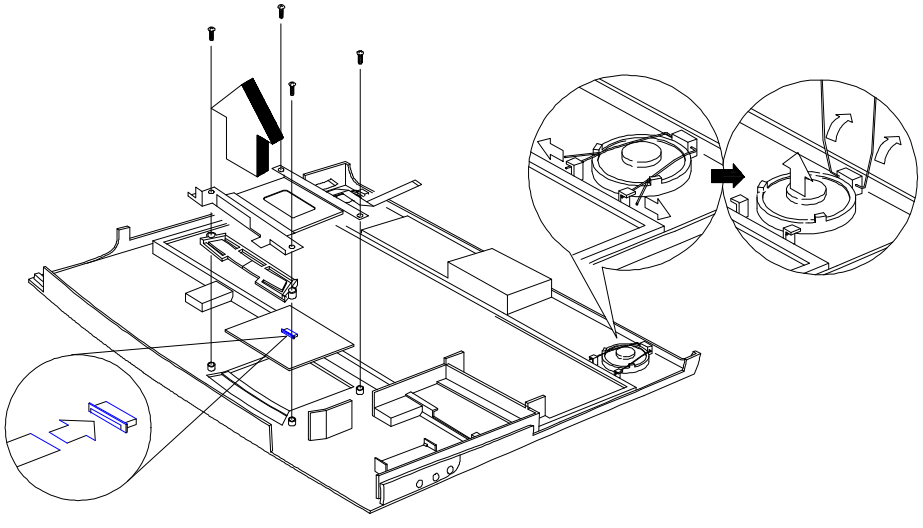


Figure 4-28 Removing the Touchpad and Speakers

4.7 Disassembling the Display

Follow these steps to disassemble the display:

1. Remove the two oval LCD bumpers at the top of the display; use a pointed instrument to remove the two mylar stickers on the bottom of the display.

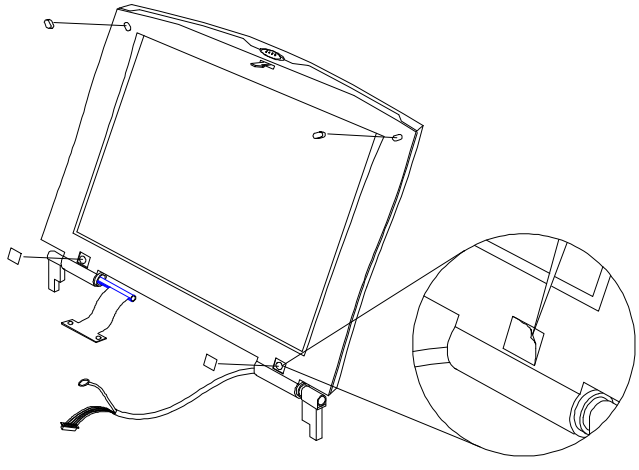


Figure 4-29 Removing the LCD Bumpers

2. Remove four screws on the display bezel.

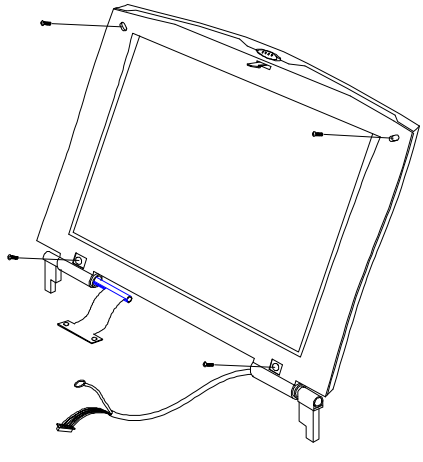


Figure 4-30 Removing the Display Bezel Screws

STN and TFT LCDs use the same bezel but different panels.

3. Pull out and remove the display bezel by first pulling on the inside of the bezel sides and lower bezel area. Then pull up the top bezel area.

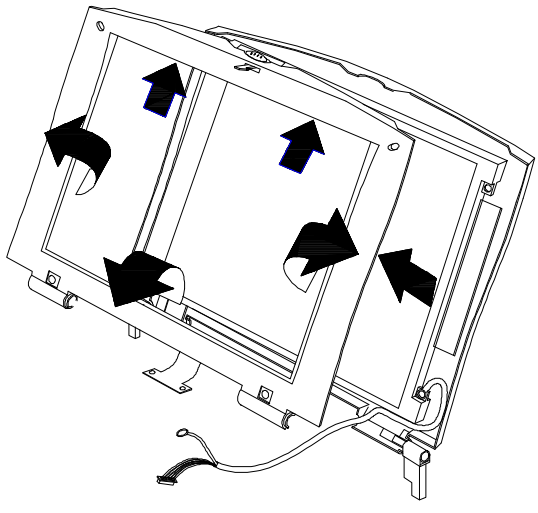


Figure 4-31 Removing the Display Bezel

4. Unplug two connectors and remove the inverter board.

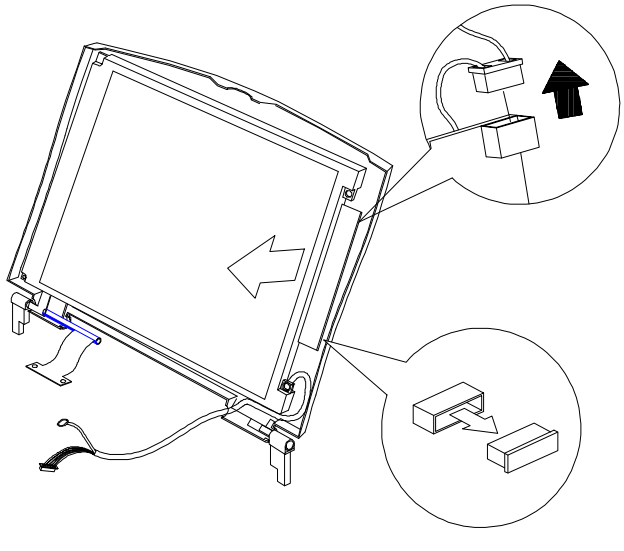


Figure 4-32 Removing the Inverter Board

5. Remove three screws on the four sides of the display panel (one screw holds and grounds the LCD cable). Then tilt the LCD Panel away for the display cover.

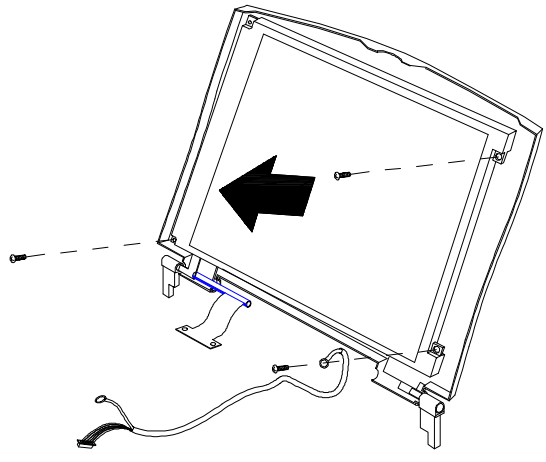


Figure 4-33 Removing the LCD Panel

Model Number Definition

This appendix shows the model number definition of the notebook.

390XX - X X X X

Brand
T: TI

Keyboard Language Versions:

0:	Swiss/US	G:	German
1:	US(110V)	I:	Italian
2:	US(220V)	J:	Japanese
3:	US w/o power cord	N:	Norwegian
4:	US K/B w/o power cord(ACLA)	R:	Russian
5:	US(110V for AAB)	S:	Spanish(220V)
6:	US(220V)with CCIB for P.R. Chinese	T:	Thailand
7:	Spanish w/o power cord	U:	UK(250V)
8:	Turkish	W:	Swedish/Finnish
A:	Arabic	X:	Swiss/German
C:	Chinese	Y:	Swiss/French
D:	Danish	K:	Korean
F:	French	Z:	w/o Keyboard

CPU/Media Bay/Memory/Battery
0: W/O CPU,W/O CD-ROM,W/O Memory,W/O Battery Uniload Model (Bulk pack)
1: P55C-166+CD-ROM+16MB RAM+Li-Ion Battery+Modem
2: P55C-166+CD-ROM+16MB RAM+Ni-MH Battery+Modem
3: P55C-150+CD-ROM+16MB RAM+Ni-MH Battery+Modem
4: P55C-133+CD-ROM+16MB RAM+Ni-MH Battery+Modem
5: P55C-133+FDD+16MB RAM+Ni-MH Battery
6: P55C-200+CD-ROM+16MB RAM+Li-Ion Battery+Modem
7: P54C-150+FDD+16 MB RAM + Ni-MH Battery

HDD:

0:	No Hard Disk	3:	340MB	A:	1GB
1:	120MB	5:	520MB	C:	1.35GB
2:	200MB	8:	810MB	D:	1.4GB/1.6GB
B:	250MB	9:	1.3GB	E:	2.0GB

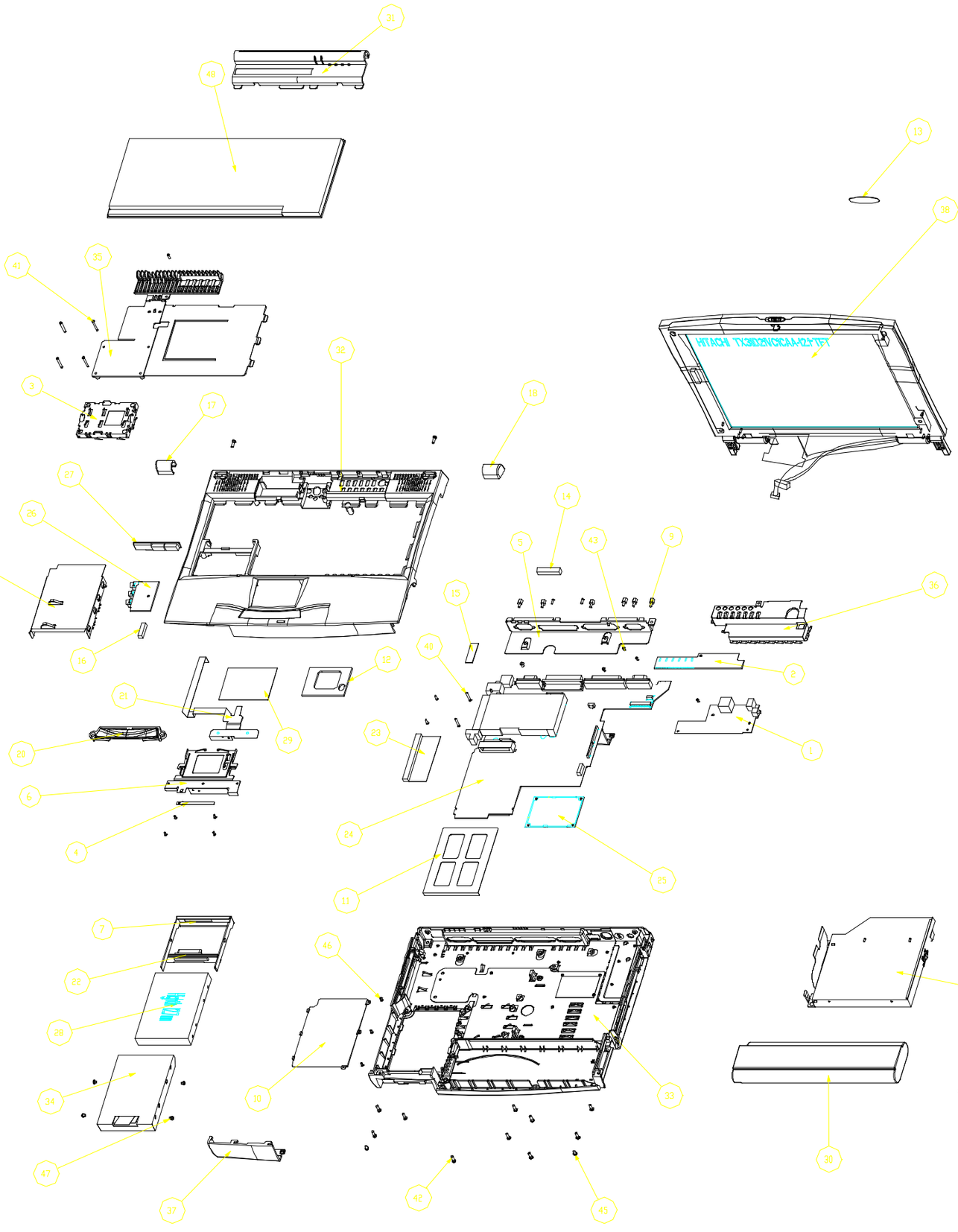
LCD:
C:12.1" SVGA DSTN
CX:12.1" SVGA TFT

Exploded View Diagram

This appendix includes exploded view diagrams of the notebook.

Table B-1 Exploded View Diagram List

No.	Description
B-1	System assembly
B-2	CD-ROM Drive assembly
B-3	LCD Module assembly
B-4	Upper Case assembly
B-5	Lower Case assembly
B-6	LCD Bezel assembly



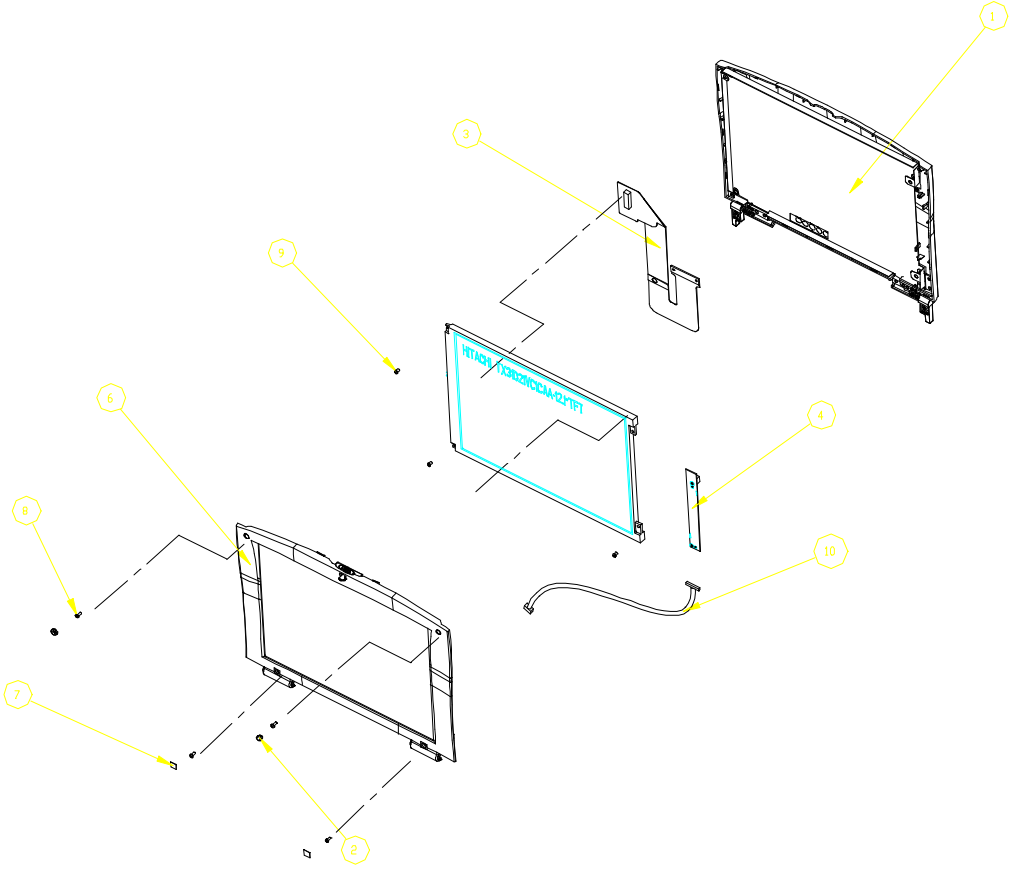
No.	PART No.	DESCRIPTION	Q'TY	REMARK
1	05.62069.020	IC CHARGER T62.069	1	
2	19.21036.001	CONVERTER DC-DC T62068	1	
3	31.42002.002	PLATE GROUND-G-IC BUCU AN750	1	
4	31.43A05.001	PLT FOR COVER SWCTOOLING) 390	1	
5	33.43A01.001	BRACKET TO AL N/A 390	1	
6	33.43A05.001	BRACKET T/P SUS N/A 390	1	
7	33.43A08.001	HOLDER HDD CONN AL N/A 390	1	
8	33.43A09.001	BRACKET HDD(TOOLING) 390	1	
9	34.00015.061	SCW HEX NYL THR-40/0#4-40 L5.5	6	
10	34.43A06.001	COVER DINN AL 050 390	1	
11	40.43A01.021	MYLAR MB FOR HDD PC N/A 390	1	
12	40.43A01.131	MYLAR FOR T/P BOARD	1	
13	40.43A02.001	PLATE NAME(LOGO) PC AN390	1	
14	42.00097.161	GASKET FOR I/O BRK	1	
15	42.00097.171	GASKET FOR RJ-11	1	
16	42.00097.181	GASKET FOR AUDIO BOARD	1	
17	42.43A03.001	COVER(L) HINGE(TOOLING) 390	1	
18	42.43A04.001	COVER(R) HINGE(TOOLING) 390	1	
19	42.43A06.001	COVER BATTERY(TOOLING) 390	1	
20	42.43A10.001	KNOB TOUCH PAD(TOOLING) 390	1	
21	50.43A03.001	C/A 8P FPC TOUCHPAD 390	1	
22	50.43A08.001	C/A 44P FPC HDD 390	1	
23	54.09011.041	MODEM CARD INTERNA T62/060/C00	1	
24	55.43A01.001	390 MAIN BOARD	1	
25	55.43A02.011	390 CPU BOARD P55C/166	1	
26	55.43A03.001	390 AUDIO BOARD	1	
27	55.43A04.001	390 KEYBOARD BOARD	1	
28	56.02759.001	HDD 2160M 2.5HIT/DK225A-21 IDE	1	
29	56.17447.061	TOUCHPA SYNA/TM3202TPD-226 050	1	
30	60.43A01.031	ASSY LI-ION BATY PACK BTP-Z3L	1	
31	60.43A05.001	ASSY MIDDLE COVER 050 390	1	
32	60.43A06.001	ASSY UPPER CASE 050 390	1	DRAWING C
33	60.43A07.001	ASSY LOWER CASE 050 390	1	DRAWING B
34	60.43A11.001	ASSY HDD PACKING BRACKET 390	1	
35	60.43A12.001	ASSY UPPER HEAT SINK 390	1	
36	60.43A13.001	ASSY EMI PLT DC-IC 390	1	
37	60.43A17.001	ASSY HDD COVER 390	1	
38	65.43A01.041	LCD ASSY MODULE(HIT TFT)	1	DRAWING B
39	65.43A02.001	ASSY CD ROM MODULE 050 390	1	DRAWING A
40	86.1A522.140	SCREW MACH PAN M2*14L NI	2	
41	86.1A522.175	SCREW MACH PAN M2*17.5L	4	
42	86.1A553.8R0	SCREW PAN NYLOK M2.5*8L B-ZN	12	
43	86.1A522.4R0	SCREW MACH PAN M2*4L NI	13	
44	86.1A522.6R0	SCREW MACH PAN M2*6L NI	11	
45	86.1A553.4R0	SCREW MACH PAN M2.5*4L	6	
46	86.1A122.4R0	SCREW MACH PAN M2*4L ZN BLACK	3	
47	86.5A524.4R0	SCREW MACH FL M3*4L NI	4	
48	90.46907.001	US KB-84 KEY KAS1901-0161R	1	

MODEL	AN390	NAME EXPLODE DRAWING	1	RELEASE DRAWING	09/26/1997
DRN	Jacky S.W. Chang	MATERIAL	REV	DESCRIPTION	SIGN DATE
DSN		FINISH	DIM IN mm	DO NOT SCALE DWG	
CKD		Acer Incorporated	SHEET 1 OF 1		
APPD			DRAWING NO.	CD 91.43A01.001	

ANG. TOL± 0°~30° 0.2° 30°~60° 0.5° 60°~90° 1°

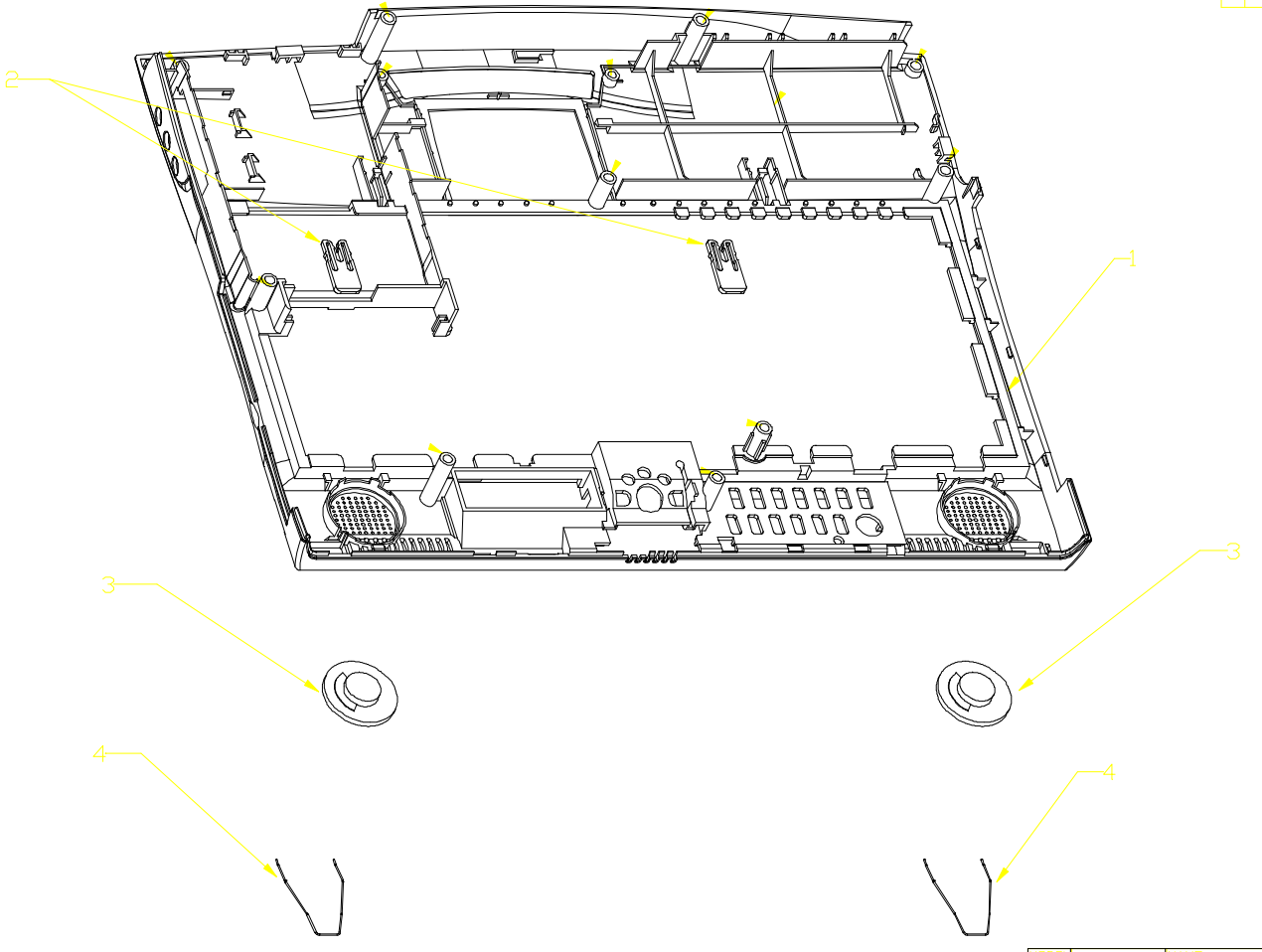
Acer

NO.	PART NO.	DESCRIPTION	Q'TY	REMARK
1	60.43A05.021	ASSY LCD PANEL (HIT TFT)	1	B-1
2	47.43A01.001	CUSHION_BEZEL	2	B-2
3	50.43A01.011	FPC_LCD_TFT	1	B-3
4	19.21030.111	INVERTER	1	B-4
5	56.07468.021	LCD HIT-TFT	1	B-5
6	60.43A04.011	LCD_BEZEL_ASSY	1	B-6
7	40.43A01.081	MYLAR_for_HINGE	2	B-7
8	86.1A553.6R0	SCREW_MACH_PAN M2.5*6L_NY	4	
9	86.4A553.6R0	SCREW_M3*6	3	
10	50.43A02.001	W.A 10P #30 220MM INVERTER 390	1	B-8



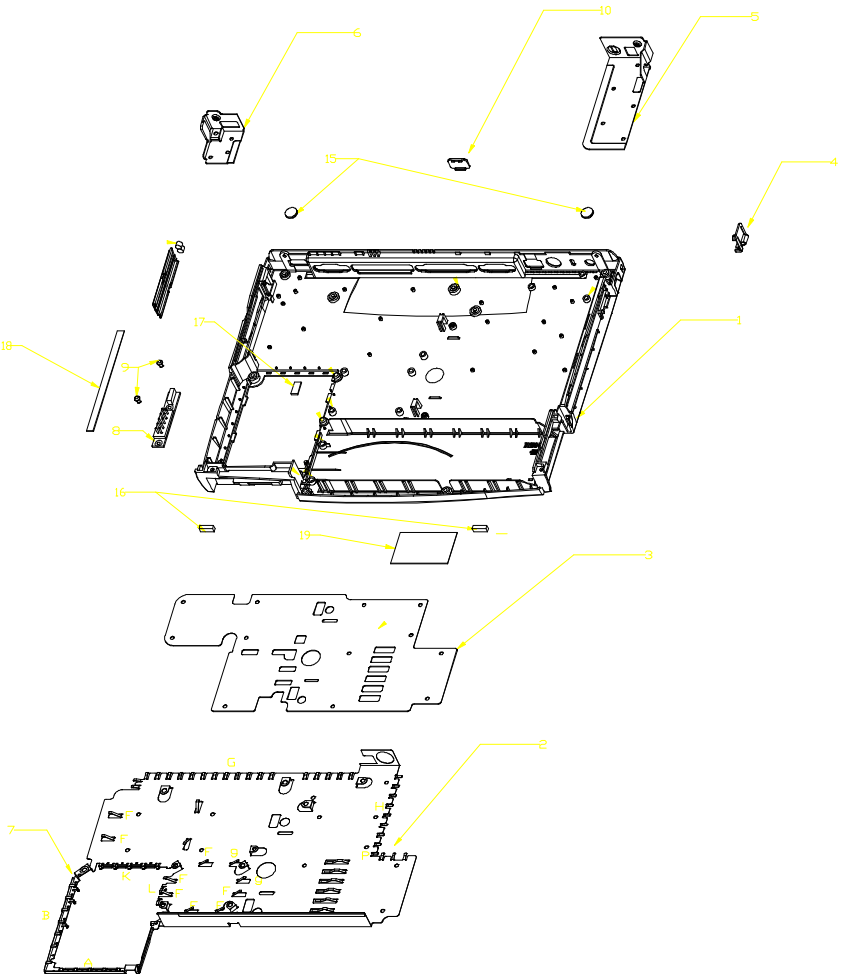
MODEL	AN390	NAME	ASSY LCD MODULE(HIT TFT)	1		DRAWING B	09/25/1997
DRN	Jacky S.W. Chang	MATERIAL		REV	ECN NO.	DESCRIPTION	SIGN / DATE
DSN		FINISH				DIM IN mm	DO NOT SCALE DWG
CKD		Acer Incorporated				SHEET OF	
APPD						DRAWING NO.	CD 653A01.041

NO.	PART NO.	DESCRIPTION	Q'TY	REV	REMARK
1	39.43A01.001	UPPER CASE	1	1	C-1
2	42.43A02.011	KB LATCH KNOB	2	1	C-2
3	23.40031.001	WIRE ASS'Y FOR SPEAKER	2	1	C-3
4	34.43A08.001	SPEAKER SPRING	2	1	C-4
5					
6					



MODEL	AN390	NAME	U-CASE ASS'Y	1	DRAWING C		09/26/1997
DRN	Jacky S.V. Chang	MATERIAL	PC/ABS, MCS-650	REV	DESCRIPTION	SIGN	DATE
DSN		FINISH			DIM IN mm	DO NOT SCALE DWG	
CKD		Acer Incorporated			SHEET 1 OF 1		
APPD					DRAWING NO.	CD 60.43A06.001	

Acer

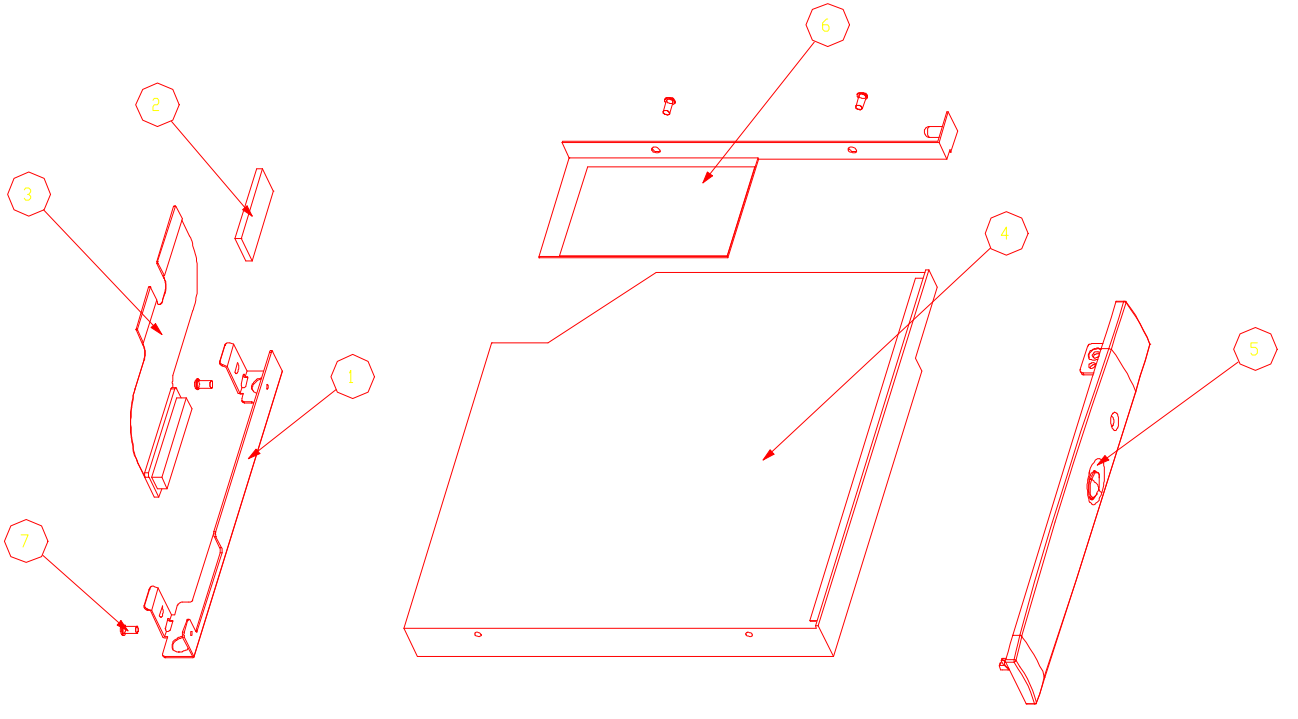


NO.	PART NO.	DESCRIPTION	QTY	REV	REMARK
1	39.43A02.001	LOWER CASE	1	1	D-1
2	31.43A07.001	L-CASE EMI PLATE	1	1	D-2
3	34.43A09.001	L-HEAT SINK	1	1	D-3
4	42.43A09.001	POWER KNOB	1	1	D-4
5	34.40A03.001	L-CASE SUPPORTING (R)	1	1	D-5
6	34.40A02.001	L-CASE SUPPORTING (L)	1	1	D-6
7	31.43A07.011	L-CASE EMI PLATE-A	1	1	D-7
8	55.43A05.001	390 BATTERY BOARD	1	1	D-8
9	B6.1A553.4R0	SCREW PAN M2.5*4L NY NI	2		
10	42.46931.001	SIR COVER	1	1	D-9
11	34.43A12.001	SPRING FOR PCMCIA	1	1	D-10
12	34.46928.001	SPRING FOR PCMCIA(L)	1	1	D-11
13	42.46913.001	DOOR,PCMCIA	1	1	D-12
14	42.46919.001	DOOR,PCMCIA(L)	1	1	D-13
15	47.45001.001	FOOT,350P	2	1	D-14
16	47.46902.001	FOOT,L-CASE(AN370)	2	1	D-15
17	34.43A01.001	TAPE COPPER	1	1	D-16
18	40.43A01.101	MYLAR LOWER CASE	1	1	D-17
19	47.43A12.001	THERMAL PAD	1	1	D-18

MODEL	AN390	NAME	LOWER CASE ASS'Y	1	DRAWING D
DRN	Jacky S.W. Chang	MATERIAL	PC/ABS, MCS-050	REV	DESCRIPTION
DSN		FINISH		DIM IN mm	DO NOT SCALE DWG
CKD		Acer Incorporated		SHEET 1 OF 1	
APPD				DRAWING NO.	CD 60.43A07.001

09/26/1997

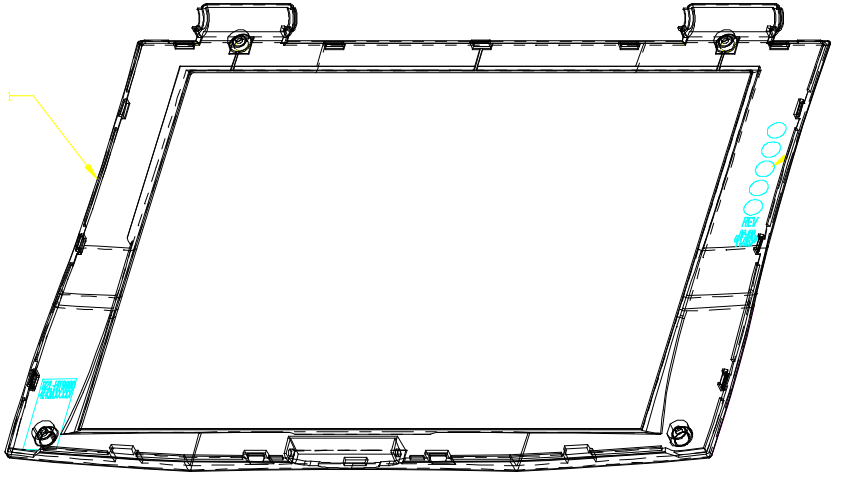
NO.	PART NO.	DESCRIPTION	Q'TY	REMARK
1	33.43A06.001	BRACKET CD SUS N/A 390	1	A-1
2	47.43A13.001	CD-ROM SPONDGE	1	A-2
3	50.43A06.001	C.A 70P FPC 60MM CD-ROM 390	1	A-3
4	56.10013.271	CD DRV MATSUS/UJDA112 14X ACER	1	A-4
5	60.43A02.001	ASSY CD-ROM BEZEL 050 390	1	A-5
6	60.43A16.001	ASSY CD-ROM HOLDER	1	A-6
7	86.1A522.4R0	SCREW MACH PAN M2*4L NI	4	

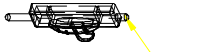


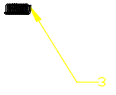
MODEL	AN390	NAME ASSY CD ROM MODULE 050 390	1	DRAWING A		09/25/1997
DRN	Jacky S.W. Chang	MATERIAL PC/ABS, MCS-050	REV	DESCRIPTION	SIGN	DATE
DSN		FINISH			DO NOT SCALE DWG	
CKD		Acer Incorporated		DIM IN mm		
APPD				SHEET 1 OF 1		
				DRAWING NO. CD 65.43A02.001		

Acer

NO.	PART NO.	DESCRIPTION	Q'TY	REV.	REMARK
1	41.43A02.001	LCD BEZEL HIT	1	0	E-1
2	42.43A01.001	LCD LATCH	1	0	E-2
3	34.47A04.001	SPRING FOR LCD LATCH	1	0	E-3
4					
5					







MODEL	AN390	NAME	LCD BEZEL HIT ASS'Y	0	DRAWING E	05/05/1997
DRN	Jacky S.W. Chang	MATERIAL	PC/ABS, MCS-050	REV.	DESCRIPTION	SIGN / DATE
DSN		FINISH			DIM IN mm / DO NOT SCALE DWG	
CKD		Acer Incorporated			SHEET 1 OF 1	
APPD					DRAWING NO.	CD 60.43A04.11

ANG TOL± 0°-30° 0.5° 60°-90° 1°

Acer

Spare Parts List

This appendix lists the spare parts of the notebook computer.

Table C-1 Spare Parts List

Category	Ref. No. of Exploded Diagram	Description	Acer Part No.	Comment/Location	Min. Qty
LCD Module	B-4	INVERTER BD	19.21030.111		5
(HIT TFT)	E-2/3	LCD PANEL LATCH PACK	6M.43A06.001	34.47604.001 SPRING * 4 + 42.43A01.001 LACTCH*2	5
	B-3	C.A 41/50P IBM12.1 TFT 170MM	50.43A01.011	LCD TO MB CABLE	20
	B-10	W.A 10P #30 220MM INVERTER 390	50.43A02.001	WIRE FOR INVERTER TO MB	50
	B-5	LCM TX31D21 12.1"TFT SVGA HIT	56.07468.021		1
	B-6	ASSY LCD BEZEL(HIT) 050 390	60.43A04.011		5
	B-2	ASSY LCD PANEL(HIT TFT)050 390	60.43A05.021	W/HINGE,DIAPER	5
		LCD MODULE KIT(HIT TFT) AN390	6M.43A01.001	(FOR 65.43A01.041)	1
(HIT DSTN)	B-4	INVERTER BD	19.21030.111		5
(HIT TFT)	E-2/3	LCD PANEL LATCH PACK	6M.43A06.001	34.47604.001 SPRING * 4 + 42.43A01.001 LACTCH*2	5
	B-3	C.A 41/50P HIT9980 STN 170MM	50.43A01.001	LCD TO MB CABLE	1
	B-10	W.A 10P #30 220MM INVERTER 390	50.43A02.001	WIRE FOR INVERTER TO MB	5
	B-5	LCM LM9980ZWCC02 12.1 DSTN HIT	56.0740A.011		1
	B-6	ASSY LCD BEZEL(HIT) 050 390	60.43A04.011		5
	B-2	ASSY LCD PANEL(HIT) 050 390	60.43A05.011		5
		ASSY LCD MODUL(HIT9981)050 390	6M.43A05.001	(FOR 65.43A01.021)	1
(SANYO DSTN)	B-4	INVERTER BD	19.21030.111		5
(HIT TFT)	E-2/3	LCD PANEL LATCH PACK	6M.43A06.001	34.47604.001 SPRING * 4 + 42.43A01.001 LACTCH*2	5
	B-3	C.A 41/50P HIT9980 STN 170MM	50.43A01.001	LCD TO MB CABLE	1
	B-10	W.A 10P #30 220MM INVERTER 390	50.43A02.001	WIRE FOR INVERTER TO MB	5
	B-5	LCD 12.1 DSTN LM-JK53-22NFR	56.0743A.011		1
	B-6	ASSY LCD BEZEL(HIT) 050 390	60.43A04.011		5
	B-2	ASSY LCD PANEL(HIT) 050 390	60.43A05.011	W/ DIAPER, HINGE SUPPORT	5
		ASSY LCD MODULE(SANYO)050 390	6M.43A04.001	(FOR 65.43A01.001)	1
Upper Case	C-4	SPK 0.5W 78DB ZK-2808C 140M	23.40031.011		5
		ASSY UPPER CASE 050 390	60.43A06.001		1

Table C-1 Spare Parts List

Category	Ref. No. of Exploded Diagram	Description	Acer Part No.	Comment/Location	Min. Qty
Lower Case	D-10 ~ D-13	PCMCIA DOOR PACK 390	6M.43A07.001	INCLUDING THE FOLLOWING PARTS	5
	D-10			34.43A12.001 SPRING PCM DOOR UPPER SUS 390 * 4PCS	
	D-11			34.46928.001 SPRING PCM DOOR_L SUS PEACH * 4 PCS	
	D-12			42.46913.001 DOOR PCMCIA ABS 050 370 *2PCS	
	D-13			42.46919.001 DOOR(L) PCMCIA ABS 050 AN370 * 2PCS	
		ASSY LOWER CASE 050 390	60.43A07.001		1
Boards		IC CHARGER T62.069	05.62069.020		1
	2	CONVERTER DC-DC T62.068	19.21036.001		1
	23	MODEM CARD INTERNA T62/060/C00	54.09011.041		1
	24	390 MAIN BOARD	55.43A01.001		1
	25	390 CPU BOARD P55C/166	55.43A02.011		1
		390 AUDIO BOARD	55.43A03.001		5
		390 KEYBOARD BD	55.43A04.001		5
		390 BATTERY BOARD	55.43A05.001		5
		AUDIO BOARD KIT FOR AN390	6M.43A02.001	55.43A03.001+ 50.43A04.001	1
Main Board		COVER LI BTY PROTECT 760I	42.46012.001		50
Components		SIR MODULE IBM31T1100	56.15445.021	U1	5
		SIR MODULE TEMIC TFDS6000	56.15470.001	U37	5
		IC AUDIO CHIPYMF715E	71.00715.E08	U20	5
		IC PCMCIA CTRL PCI125GFN V.A	71.01250.B0U		1
		IC CLK GEN MK1422 SO-N 8P	71.01422.00A	U28	5
		IC CLK GEN CY2272 SSOP 48P	71.02272.00I	U39	5
		IC RTC BQ3285LD SSOP 24P	71.03285.B0I		5
		IC SUPER I/O FDC37672 V.B TQFP	71.37672.B0G	U17	5
		IC GUI ACCEL. 65555 V2.0 BGA	71.65555.B0U	U24	1
		IC CHIP M1531B V. C BGA	71.M1513.BDU	U41	5
		IC BUS BR1 M1533 A1-F BGA	71.M1533.F0U	U35	5
		IC SRAM 61L6432E-7 32K*64 TQFP	72.06432.00G	U44	5
		IC DRAM 256K*16-50 EDO3.3 TSOP	72.16258.029	U4 6 16 26	5
		IC SRAM W24L257AJ-15 32K*8 SOJ	72.24257.00B	U45	50
		IC EPROM 28F020 150NS 2M PLCC	72.28020.063	U7	1
		IC DRAM 256K*16-50 EDO3.3 TSOP	72.63163.029	U4 6 16 26	5
		IC AUDIO AMP LM4863 SO-N 16P	74.04863.011	U27	5
		IC MASKROM M38813-057 QFP PEAC	85.46901.001	U34	5

Table C-1 Spare Parts List

Category	Ref. No. of Exploded Diagram	Description	Acer Part No.	Comment/Location	Min. Qty
Memory		DIMM EDO 16MB 3.3V 60NS	55.46804.011		1
		DIMM EDO 32MB 3.3V 60NS 4K	55.46804.021		1
		DIMM EDO 32MB 3.3V 60NS	55.46804.031		1
Keyboard		KAS1901-0184R 050 SWISS	90.46907.000		1
		KB-84 KEY KAS1901-0161R US 370	90.46907.001		1
		KAS 1901-0-0166R 050 US/A	90.46907.005		1
		KAS 1901-0167R 050 ARABIA	90.46907.00A		1
		GER KEYBD 9805758-0003 PEACH	90.46907.00G		1
		KAS1901-0162R 050 HEB	90.46907.00H		1
		KAS1901-0165R 050 THAI	90.46907.00L		1
		KAS1901-0168R 050 RUSSIA	90.46907.00R		1
		KAS1901-0190R 050 TURKISH	90.46907.00T		1
		KAS1901-0191R 050 BELGIN	90.46907.01B		1
		KAS1901-0164R 050 CHINESE	90.46907.01C		1
		KAS 1901-0187R 050 DANISH	90.46907.01D		1
		KAS1901-183R 050 FRENCH	90.46907.01F		1
		85 KAS1901-0182R 050 GEM	90.46907.01G		1
		KAS1901-0186R 050 ITALIAN	90.46907.01I		1
		KEYBD-88 KAS1901-0156R(J) 370	90.46907.01J		1
		KAS1901-0163R 050 KOREA	90.46907.01K		1
		KAS1901-0188R 050 NORWAY	90.46907.01N		1
		85 KAS1901-0192R 050 PORT	90.46907.01P		1
		KAS1901-0181R 050 SPANISH	90.46907.01S		1
		KAS1901-0181R 050 UK	90.46907.01U		1
		KAS1901-0185 050 SWEDEN	90.46907.01W		1
HDD		HOLDER HDD CONN AL N/A 390	33.43A08.001	FOR HDD	50
		C.A 44P FPC HDD 390	50.43A08.001	FOR HDD	5
		HDD 2160MB 2.5"HIT/DK225A-21	56.02759.001		1
		HDD 1440MB IBM/DMCA-21440 ATA	56.02921.001		1
		HDD 1620M 2.5" IBM/DDLA	56.02921.021		1
		HDD 2160MB IBM/DTNA-22160	56.02941.011		1
		ASSY HDD PACKING BRACKET 390	60.43A11.001	HDD BRACKET	5
FDD		C.A 25/26P 2C 320MM FDD NEW	50.47605.011	EXT. FDD CABLE	5
		FDD 1.44 3.5" D353F2 000(3MODE	56.01051.071	(MITSUMI)	1
		FDD 1.44 3.5" D353F2 000 3MODE	56.01051.072		1
		FDD EXTERNAL 370	91.46905.012		1
CD-ROM	A-5	BZL CD-ROM(TOOLING) 390	41.43A04.001	CD-ROM BEZEL	10
	A-3	C.A 70P FPC 60MM CD-ROM 390	50.43A06.001	CABLE FOR CD-ROM	5
	A-4	CD DRV MATSUS/UJDA112 14X ACER	56.10013.271		1
	A-4	CD DRV PANAS/UJDA110 14X	56.10016.211	PANASONIC	1
		CD-ROM SYS UTIL NB060 PACK 390	90.43A39.001		5

Table C-1 Spare Parts List

Category	Ref. No. of Exploded Diagram	Description	Acer Part No.	Comment/Location	Min. Qty
		INTERNAL CD-ROM DRIVE KIT 390	91.43A28.003		1
Touchpad		PLT FOR COVER SW(TOOL) 390	31.43A05.001	IN BRACKET	50
		BRACKET T/P SUS N/A 390	33.43A05.001		50
		KNOB TOUCH PAD (TOOLING) 390	42.43A10.001		50
		C.A 8P FPC TOUCHPAD 390	50.43A03.001	TOUCHPAD CABLE	5
		TOUCHPAD SYNA/TM3202TPD-226 50	56.17447.061		5
Adapter		ADT 90-264V ADP-45GB V.E3 370P	25.10046.131		1
Battery		COVER BATTERY(TOOLING) 390	42.43A06.001	BATTERY COVER	50
		ASSY NI-MH BATY PACK BTY-031	60.43A01.021	NI-MH	1
		ASSY LI-ION BATY PACK BTY-Z31	60.43A01.031	LI - ION	1
Microphone		MICROPHONE EM-83	23.42008.021		5
		CORD SPT-2 #18*2C 7A125V1830MM	27.01618.001	MICROPHONE CORD	5
Others		COVER DIMM AL 050 390	34.43A06.001	DIMM COVER	5
		* PLATE NAME(LOGO) PC AN390	40.43A02.001	ACER LOGO	50
		* PLT NAME(EXTENSA 390) 050 390	40.48406.091	EXTENSA LOGO	50
		HINGE COVER (R+L) PACK 390	6M.43A08.001	42.43A03.001 L SIDE + 42.43A04.001 R SIDE * 5 PCS	5
		C.A 4P #26 2000MM(TEL) 970	50.46813.001	TEL CABLE	50
		SCREW PACK FOR AN390	6M.43A03.001	(5 PCS FOR EACH)	5
		SYSTEM UTILITY PACK (CD)	90.43A39.001		
1. Prices subject to change without notice.					
2. The " * " items only available on mass production period.					

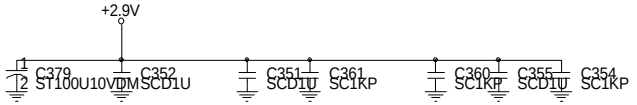
Schematics

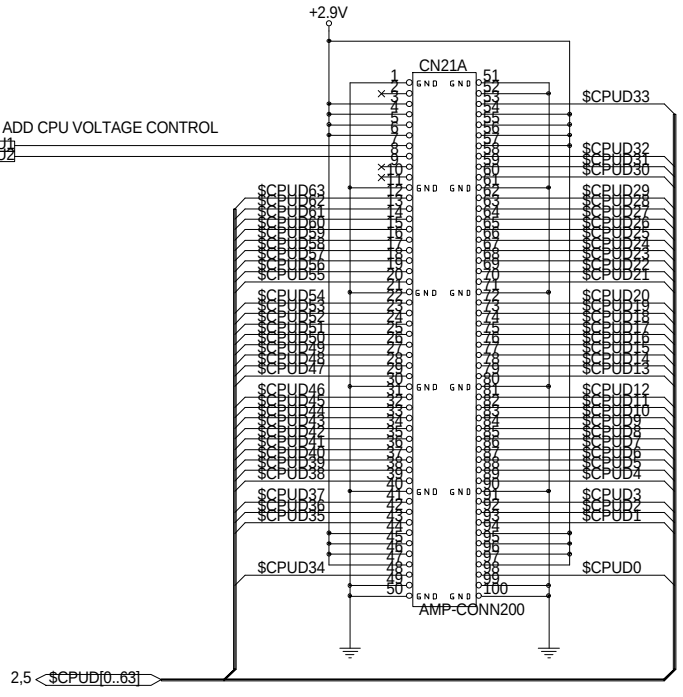
This appendix shows the schematic diagrams of the notebook.

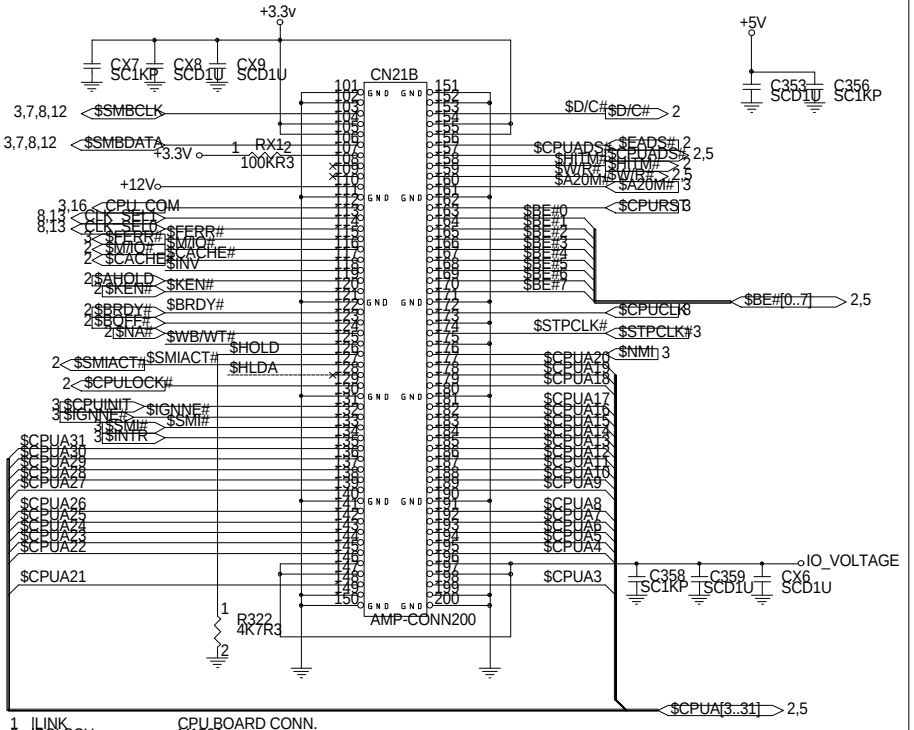
Table D-1 Schematics List

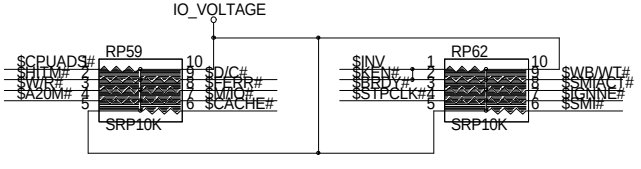
No.	Description
D-1	CPU Connector
D-2	M1531
D-3	M1533
D-4	ISA Pull High and Pull Low
D-5	Cache RAM and TAG RAM
D-6	DIMM Socket 1
D-7	DIMM Socket 2
D-8	CY2272 Clock Generator
D-9	VGA Controller Chip 65555 and VRAM
D-10	CRT and LCD Connector
D-11	PCMCIA Controller Chip PCI 1250
D-12	PCMCIA Socket and Power Controller TPS2206
D-13	M38813 and LED and Charger SMBUS
D-14	Super I/O SMC672 and RS232 MAX3243
D-15	Parallel and Serial Port
D-16	USB and FIR and Buzzer and Fan
D-17	Audio Chip YMF715
D-18	OP AMP LM4863 and Datarace and Jack
D-19	RTC and BIOS ROM
D-20	IDE Connector
D-21	Golden Finger and Modem Connector
D-22	DC-DC and Charger and Battery Connector
D-23	Port Replicator

CPU BD TO BD CONNECTOR



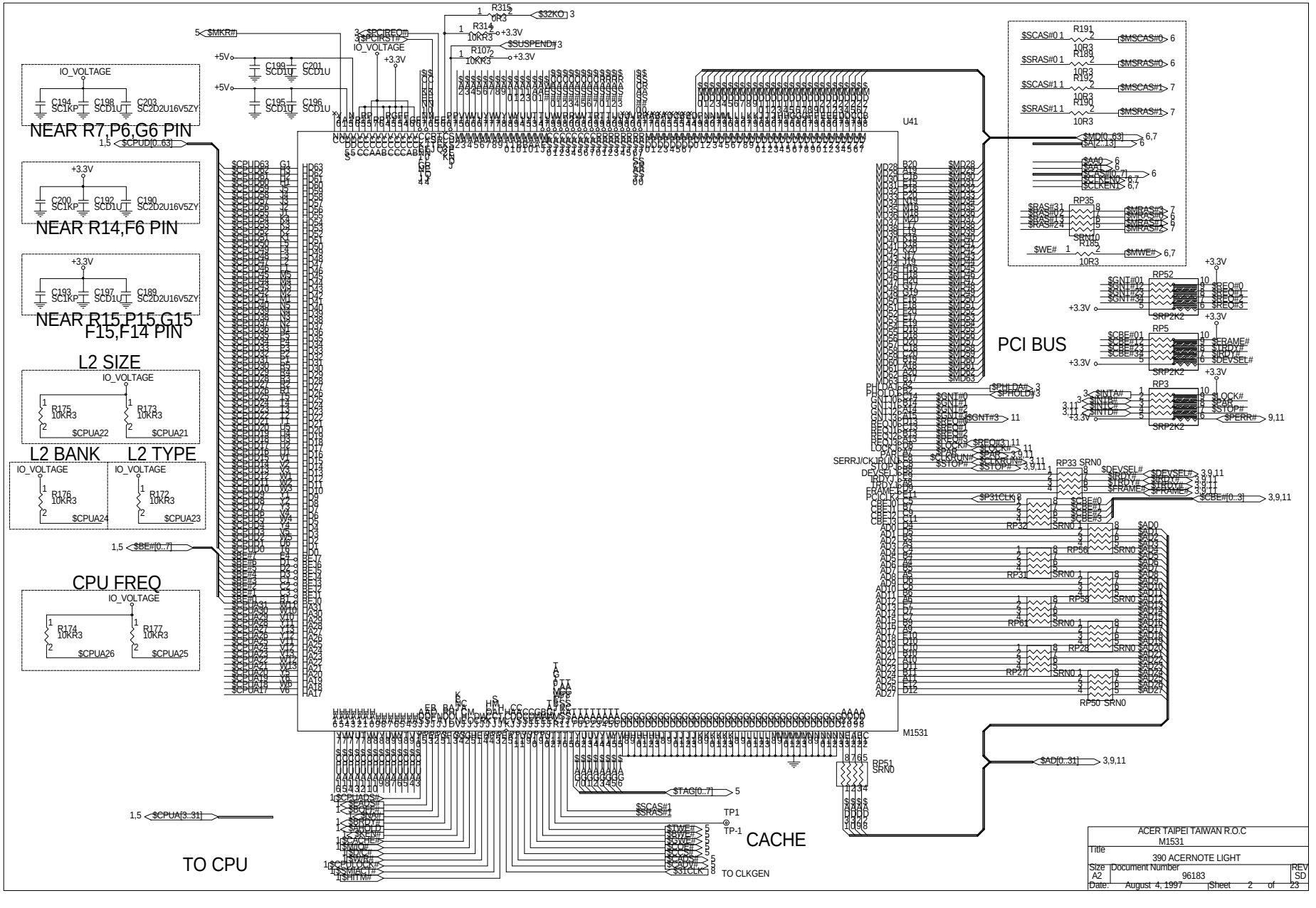


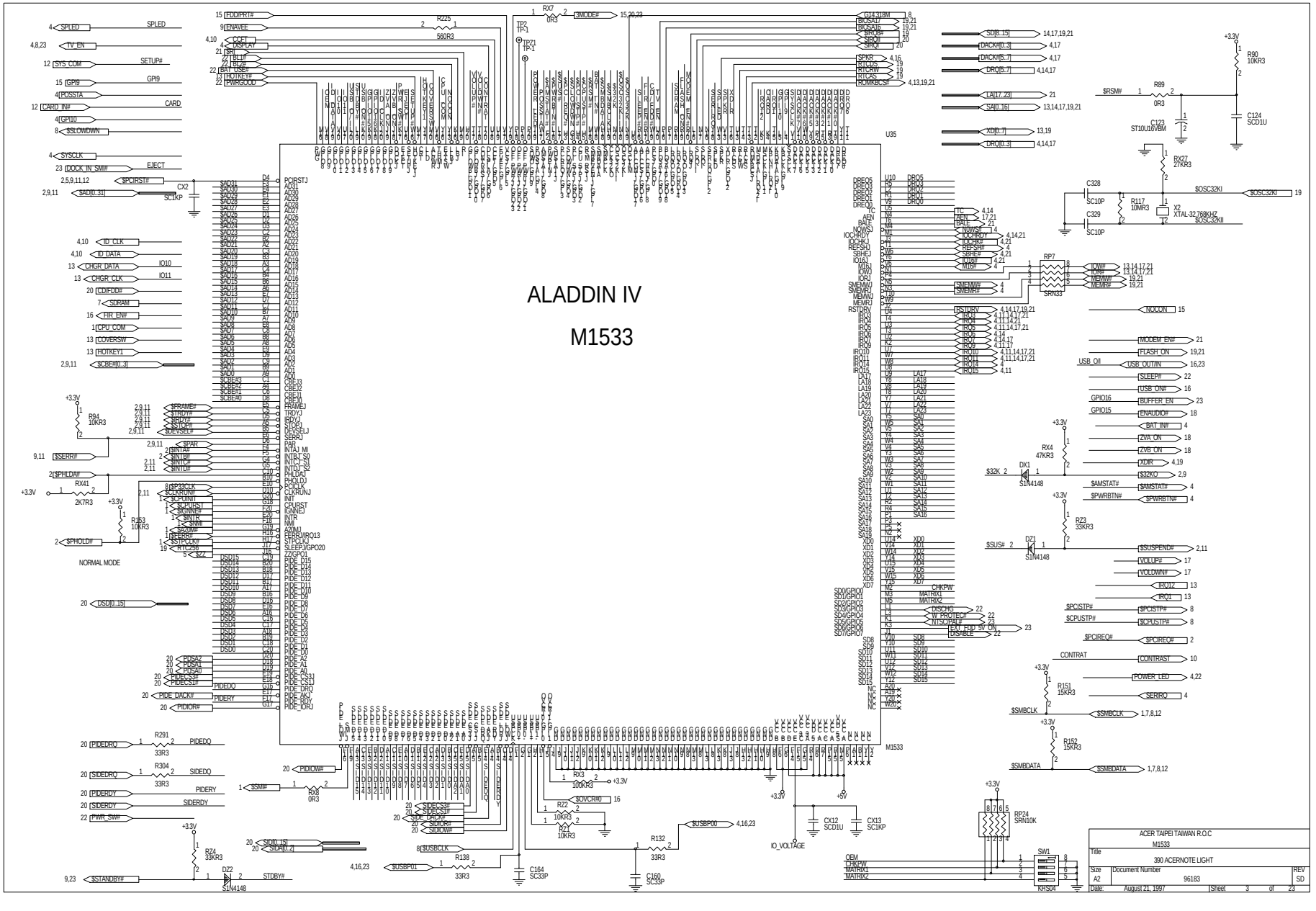




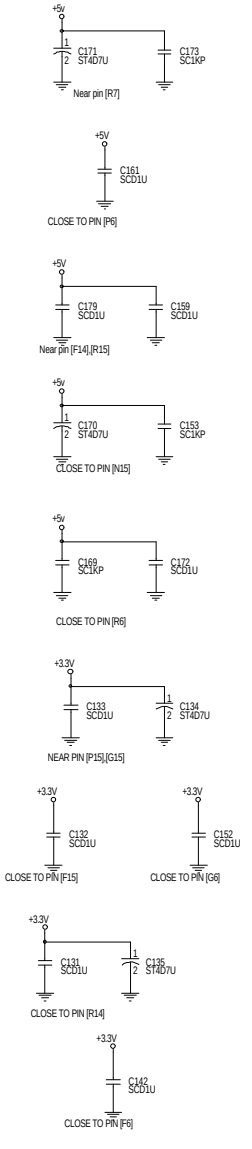
1	LINK	CPU BOARD CONN.
2	PCI.SCH	M1531
3	ISA.SCH	M1533
4	ISA_1.SCH	M1533 BYPASS CAP&PULL HIGH RISSITOR
5	CACHE.SCH	CACHE RAM & TAG RAM & AVAILABLE TTL GATE
6	DIMM1.SCH	DIMM SOCKET#1
7	DIMM2.SCH	DIMM SOCKET#2
8	CLKGEN.SCH	CLOCK GEN CY2272
9	VGA.SCH	65555 VGA CONTROLLER CHIP
10	VIDEO.SCH	CRT&LCD CONN
11	PCI1250.SCH	PCI1250 PCMCIA CONTROLLER CHIP
12	PWCON.SCH	TPS2206 PCMCIA POWER CONTROL & SOCKET
13	KBC.SCH	KB CONTROLLER 38813 CHIP
14	SIO.SCH	SUPER IO SMC37C672 & MAX3243
15	PORT.SCH	PARELL PORT&SERIAL PORT
16	USB.SCH	USB&FIR&CAN CONTROLL&BUZZER
17	AUDIO.SCH	AUDIO CHIP YMF715
18	AUDIO_1.SCH	AUDIO AMP LM4863
19	RTCROM.SCH	RTC/BIO3285&FLASH ROM
20	IDE.SCH	HDD&CD_ROM&INTERNAL FDD CONN
21	FINGER.SCH	GOLD FINGER & MODEM MODULE
22	POWER.SCH	CHARGER & DC-DC & BAT CONN
23	DOCK.SCH	PORT REPLICATOR

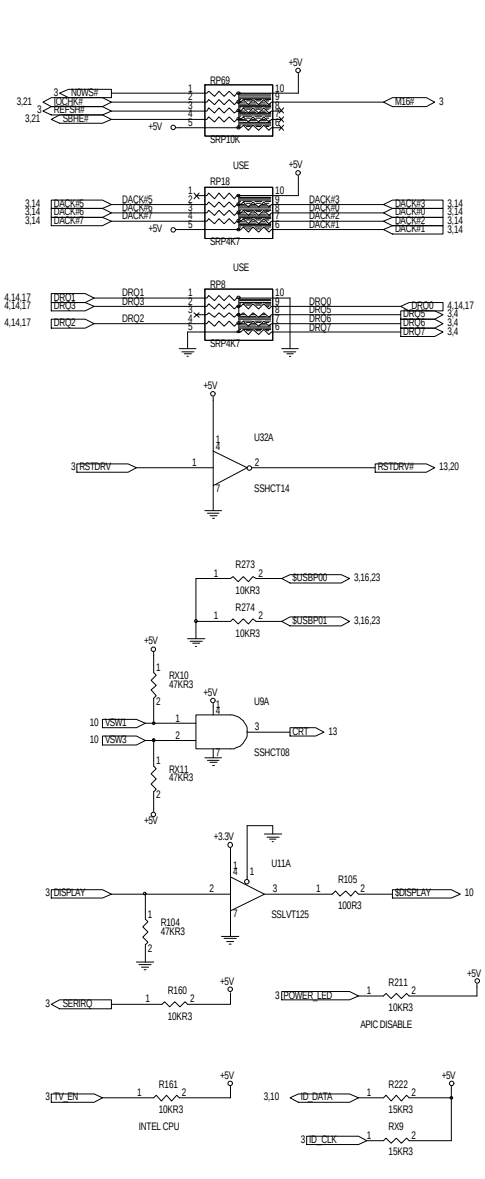
ACER TAIPEI TAIWAN R.O.C			
CPU CONN			
Title	390 ACERNOTE LIGHT		
Size	Document Number		REV
A3	96183		SD
Date:	August 5, 1997	Sheet 1 of	23

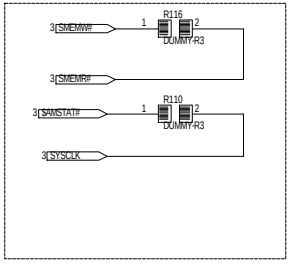

NEAR R7,P6,G6 PIN
NEAR R14,F6 PIN
NEAR R15,P15,G15
F15,F14 PIN
L2 SIZE
L2 BANK
L2 TYPE
CPU FREQ
IO_VOLTAGE
PCI BUS
CACHE
TO CPU
TO CLKGEN
U41
M1531
ACER TAIPEI TAIWAN R.O.C
M1531
390 ACERNOTE LIGHT
Size A2
Document Number 96183
REV SD
Date: August 4, 1997
Sheet 2 of 23

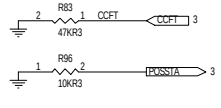

ALADDIN IV
M1533

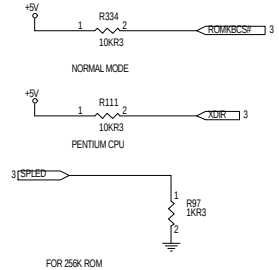
M1533 BYPASS CAPACITORS

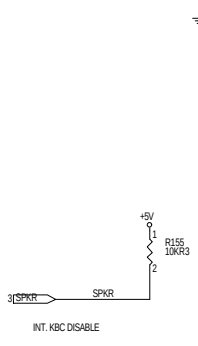


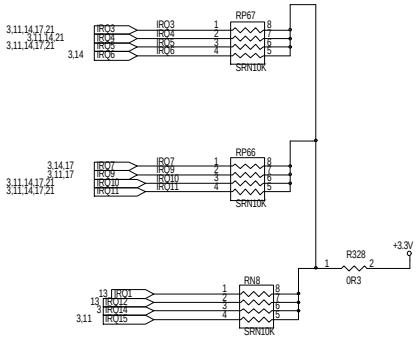


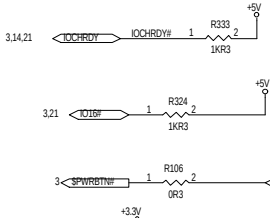








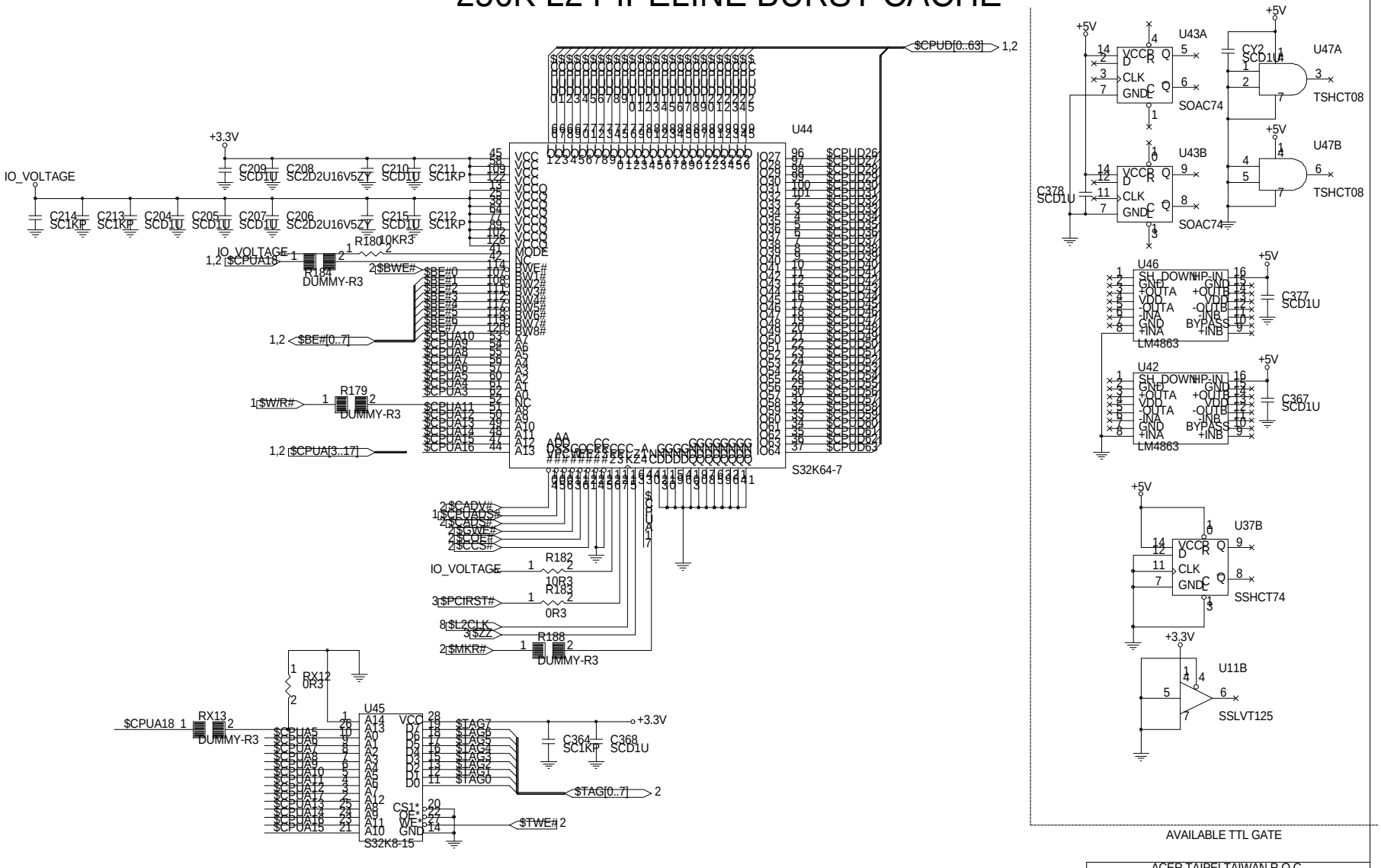




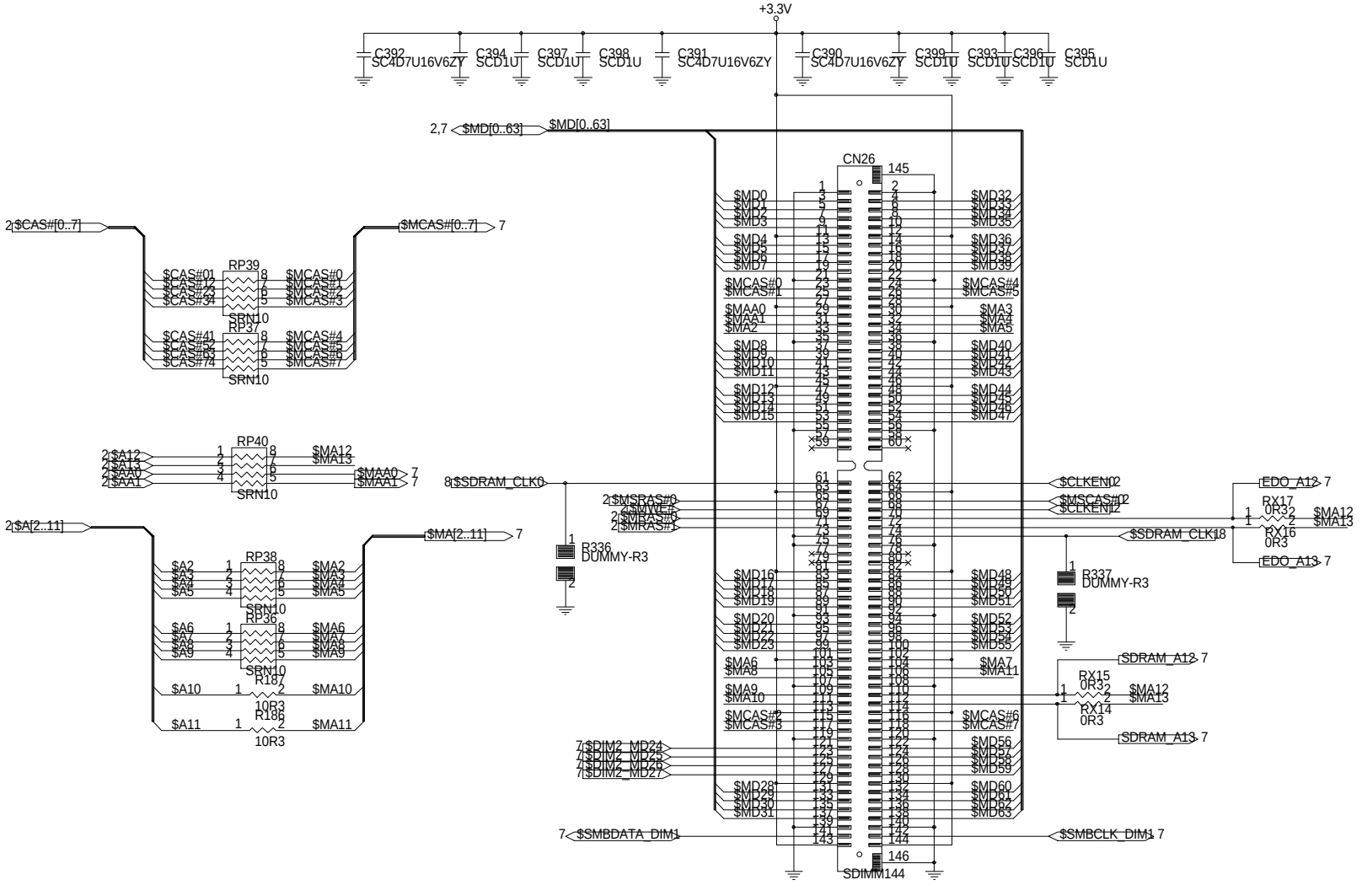
PULL HIGH	NORMAL CACHE
PULL LOW	DRAMCACHE

ACER TAIPEI TAIWAN R.O.C		
ISA PULL HIGH & PULL LOW		
Title: 390 ACERNOTE LIGHT		
Size: A2	Document Number: 96183	REV: SD
Date: August 7, 1997	Sheet 4 of 23	

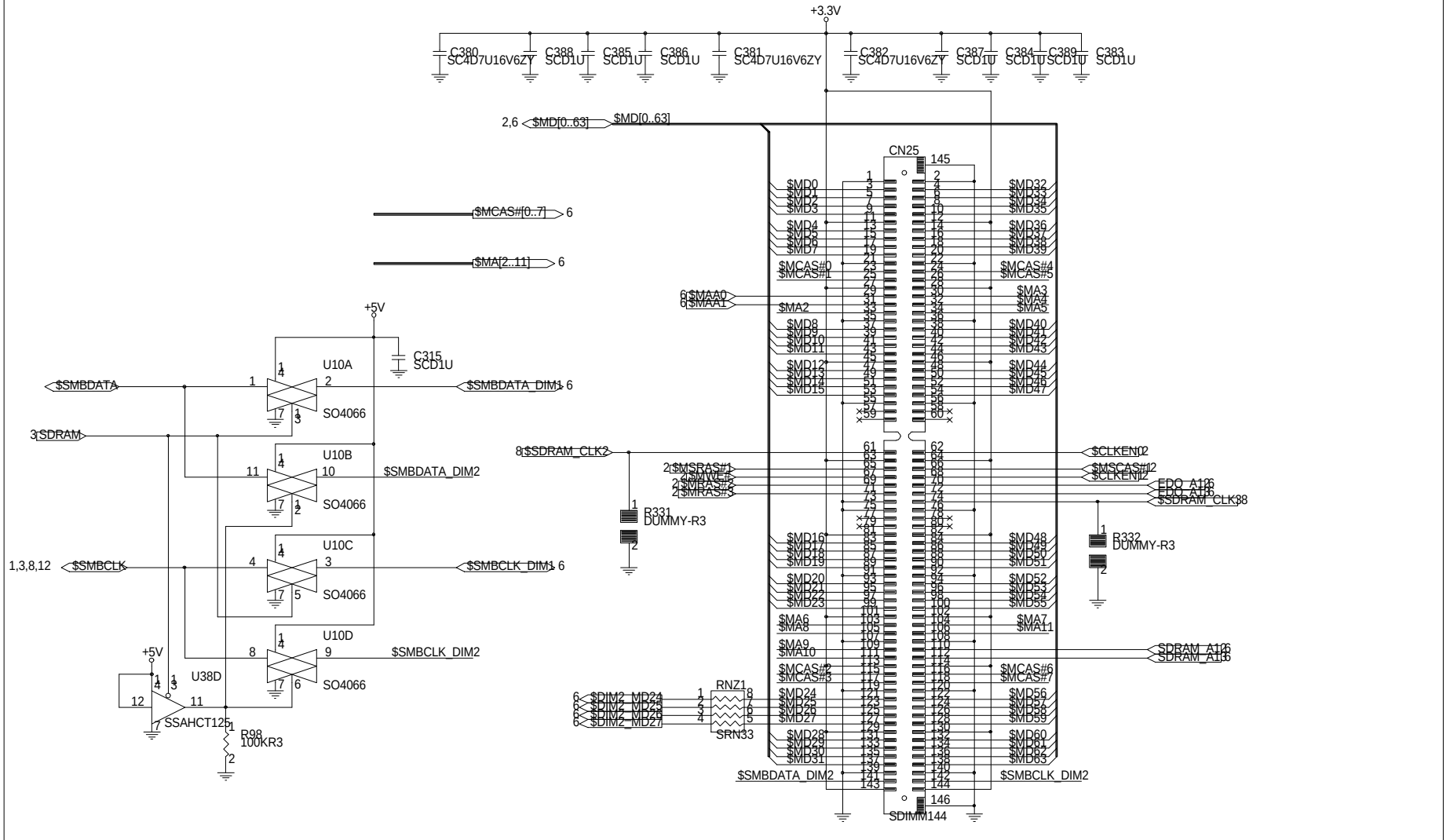
256K L2 PIPELINE BURST CACHE



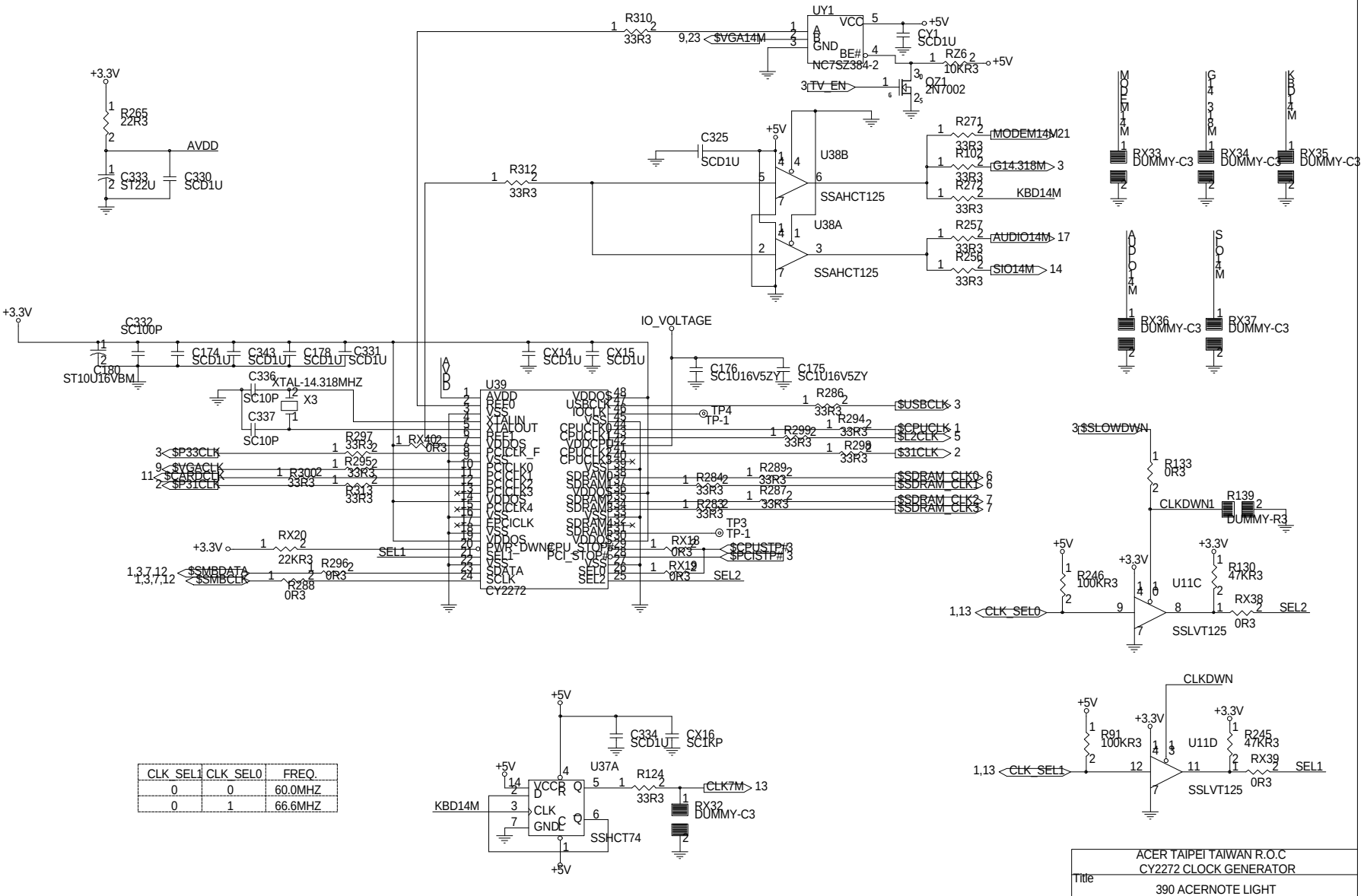
ACER TAIPEI TAIWAN R.O.C		
CACHE RAM & TAG RAM		
Title: 390 ACERNOTE LIGHT		
Size: A3	Document Number: 96183	REV: SD
Date: August 21, 1997	Sheet 5 of 23	



ACER TAIPEI TAIWAN R.O.C			
DIMM SOCKET-1			
Title	390 ACERNOTE LIGHT		
Size A3	Document Number 96183		REV SD
Date: August 4, 1997	Sheet 6 of 23		

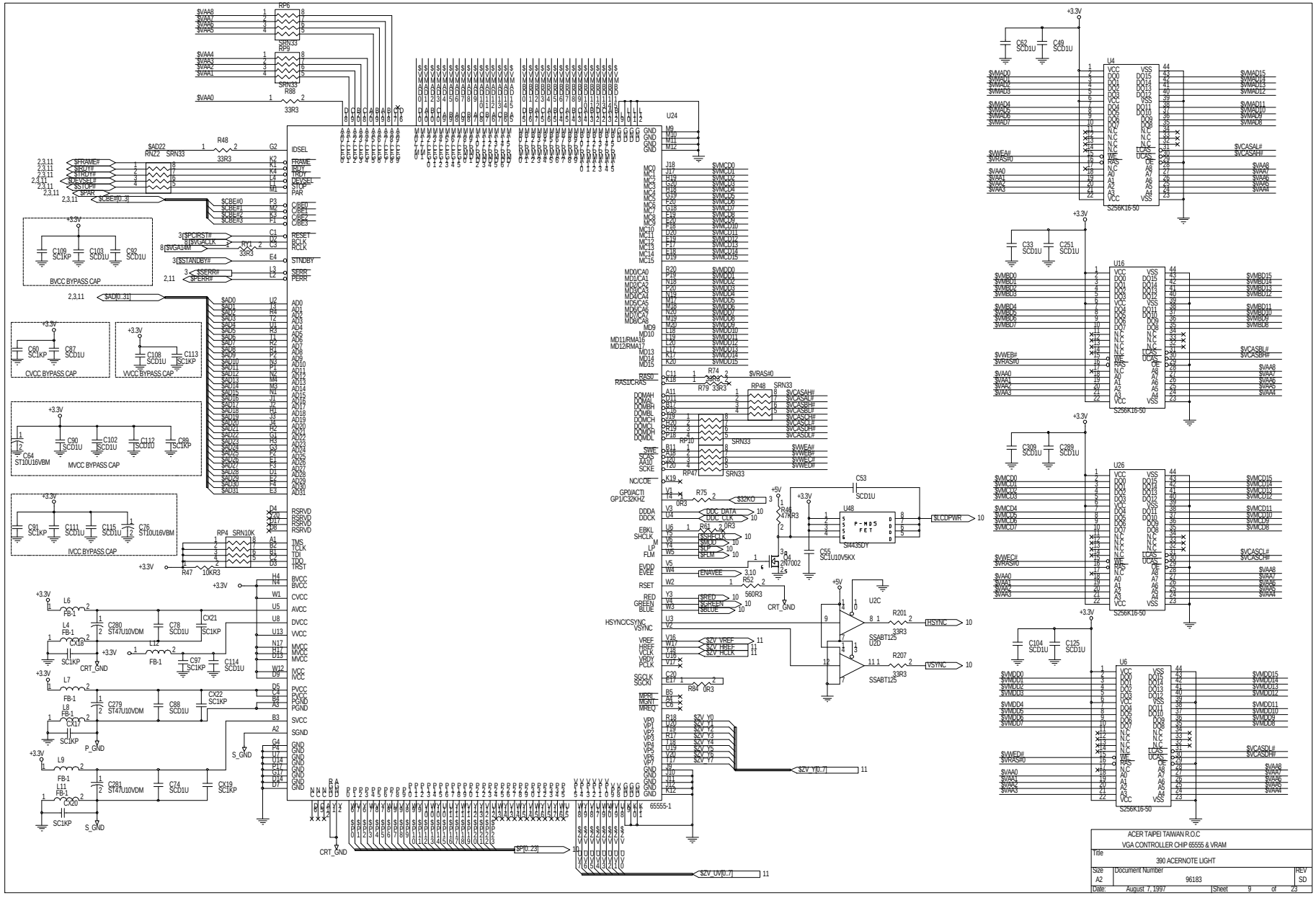


ACER TAIPEI TAIWAN R.O.C			
DIMM SOCKET-2			
Title	390 ACERNOTE LIGHT		
Size A3	Document Number 96183		REV SD
Date: August 7, 1997	Sheet 7 of 23		



CLK_SEL1	CLK_SEL0	FREQ.
0	0	60.0MHZ
0	1	66.6MHZ

ACER TAIPEI TAIWAN R.O.C
CY2272 CLOCK GENERATOR
Title
390 ACERNOTE LIGHT
Size A3 | Document Number 96183 | REV SD
Date: August 7, 1997 | Sheet 8 of 23



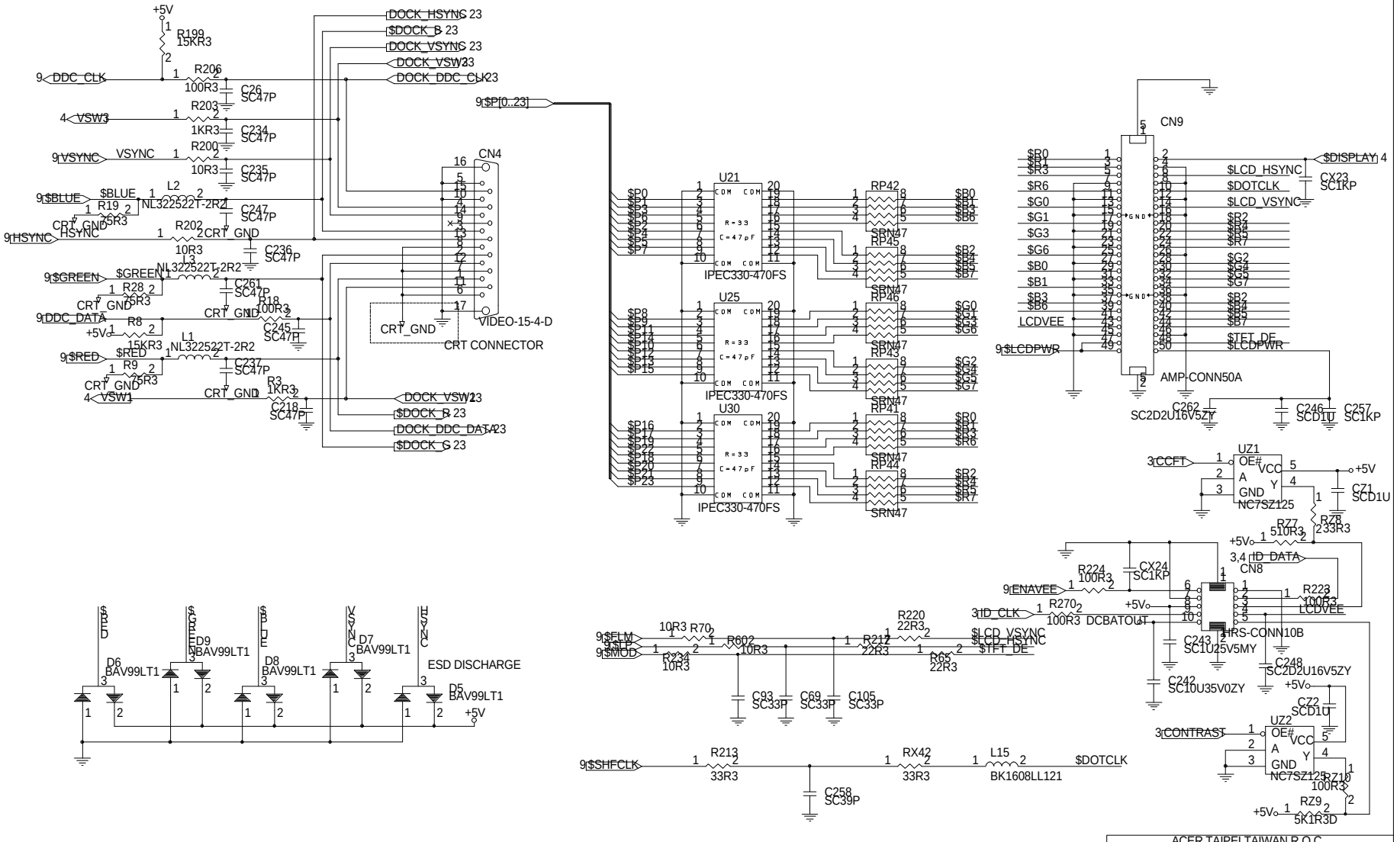
ACER TAIPEI TAIWAN R.O.C

VGA CONTROLLER CHIP 65555 & VRAM

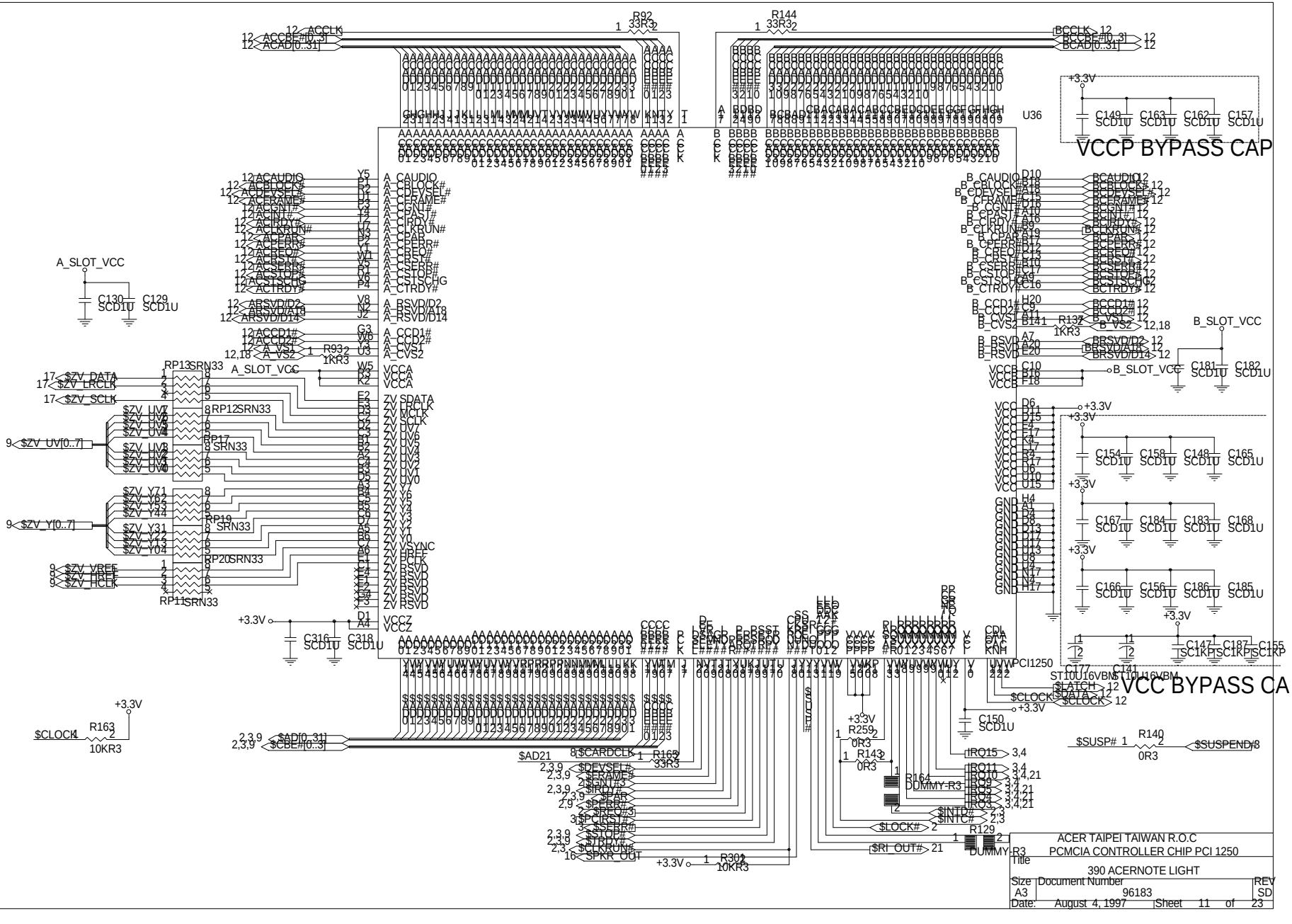
Title: 390 ACERNOTE LIGHT

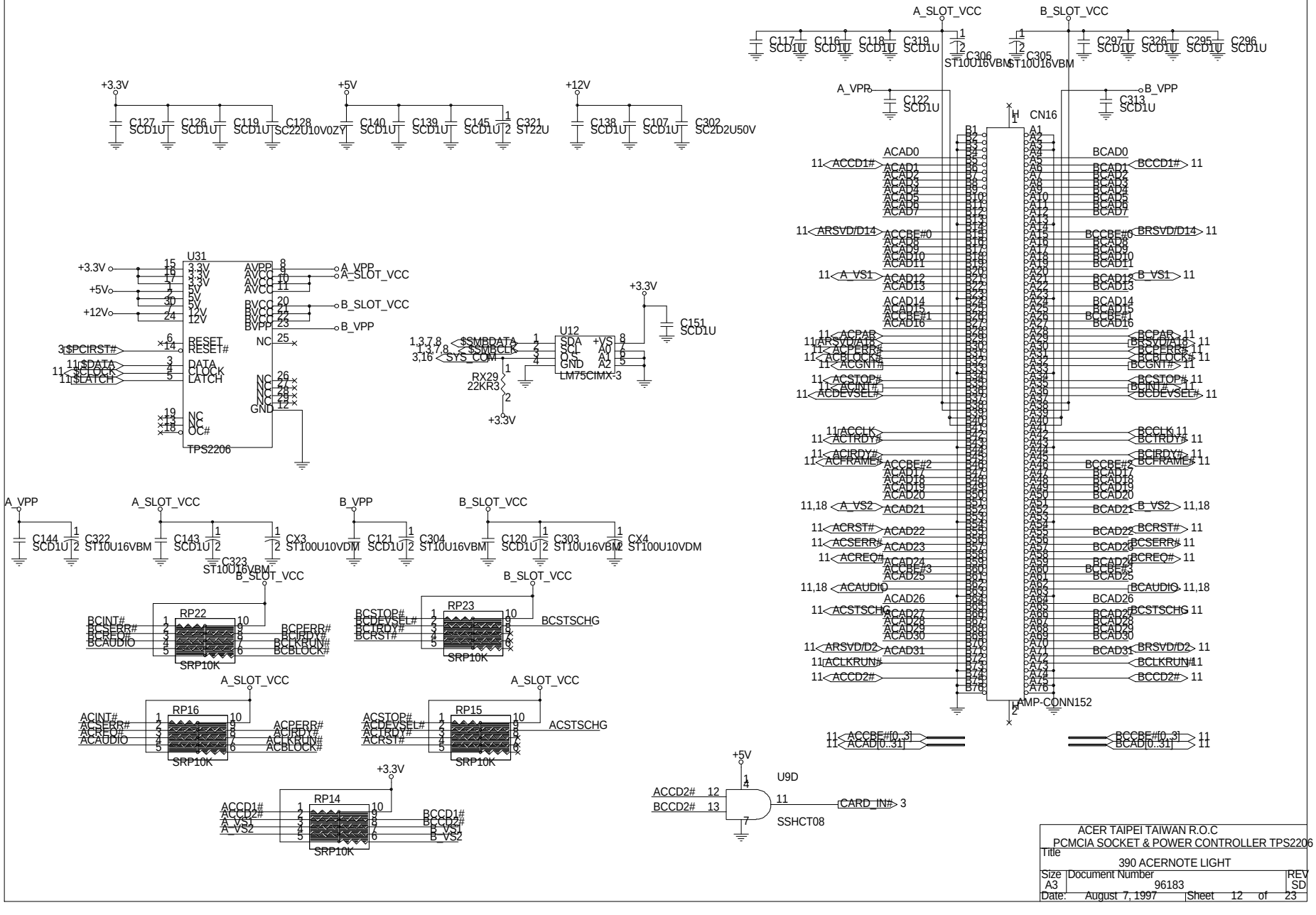
Size	Document Number	REV
A2	96183	SD

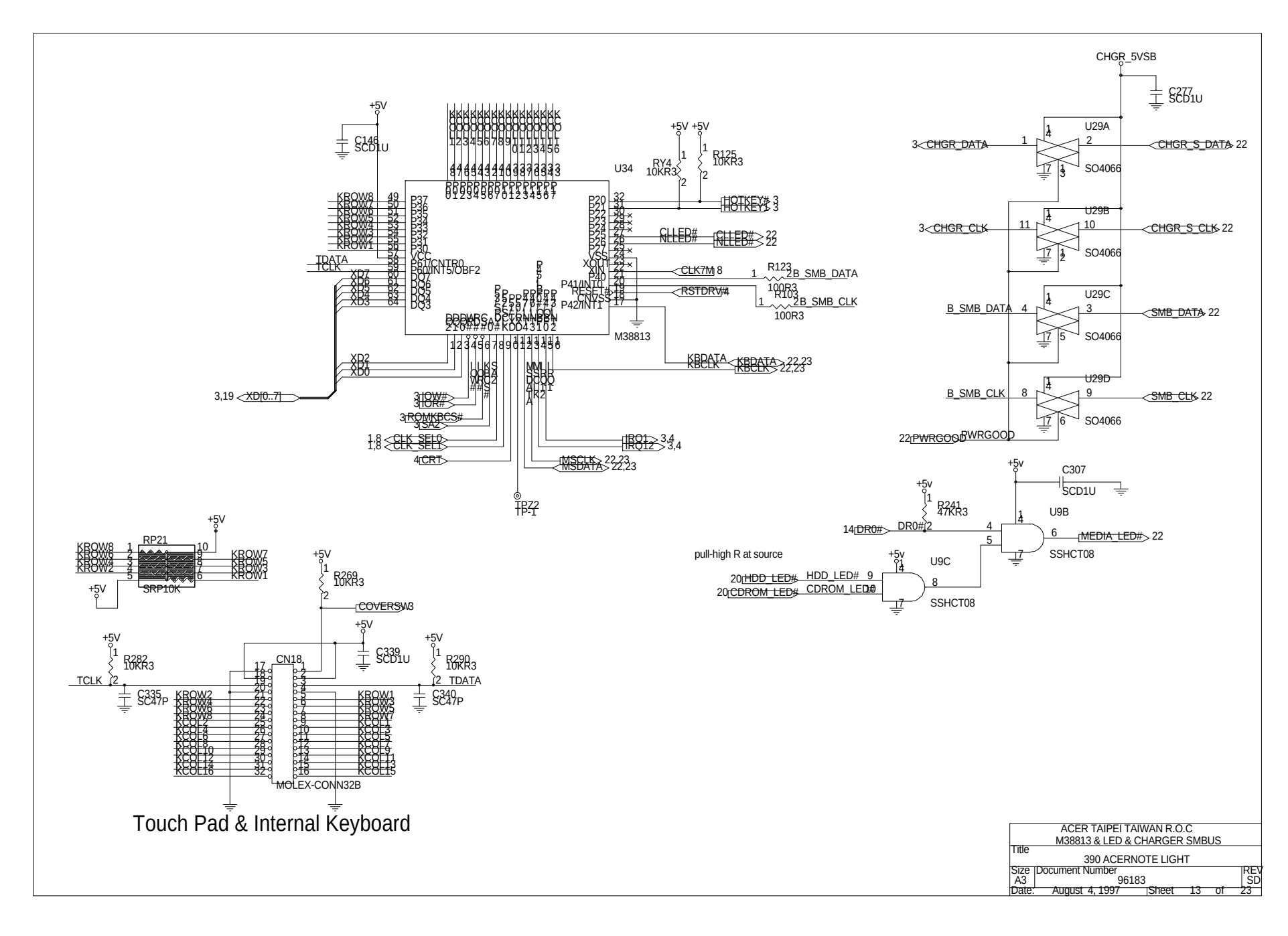
Date: August 7, 1997 | Sheet 9 of 23



ACER TAIPEI TAIWAN R.O.C		
CRT & LCD CONN		
Title	390 ACERNOTE LIGHT	
Size A3	Document Number 96183	REV SD
Date: August 21, 1997	Sheet 10 of 23	

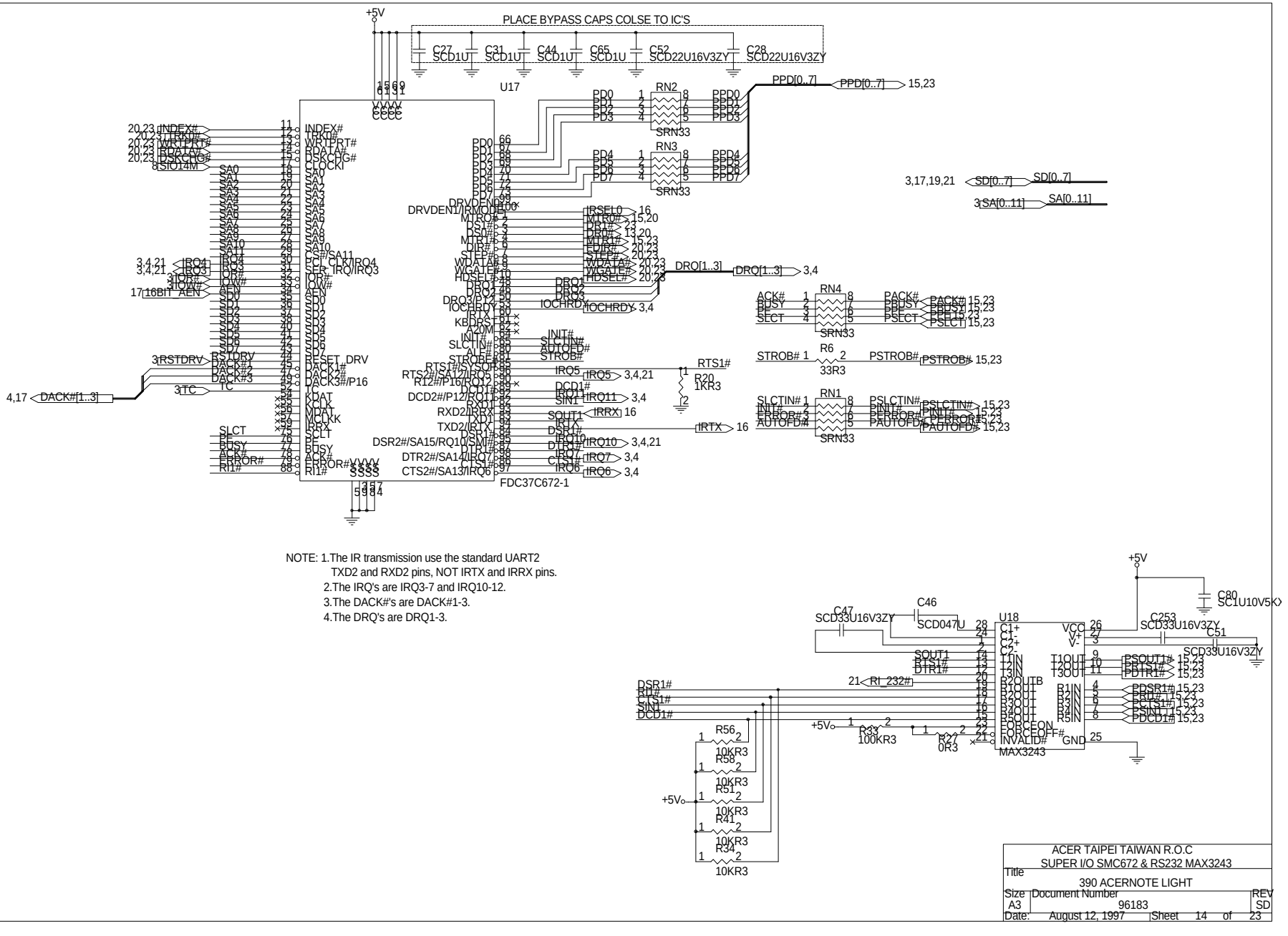

VCCP BYPASS CAP
VCC BYPASS CA
U36
A_SLOT_VCC
B_SLOT_VCC
+3.3V
ACER TAIPEI TAIWAN R.O.C
PCMCIA CONTROLLER CHIP PCI 1250
Title
390 ACERNOTE LIGHT
Size A3
Document Number 96183
REV SD
Date: August 4, 1997
Sheet 11 of 23

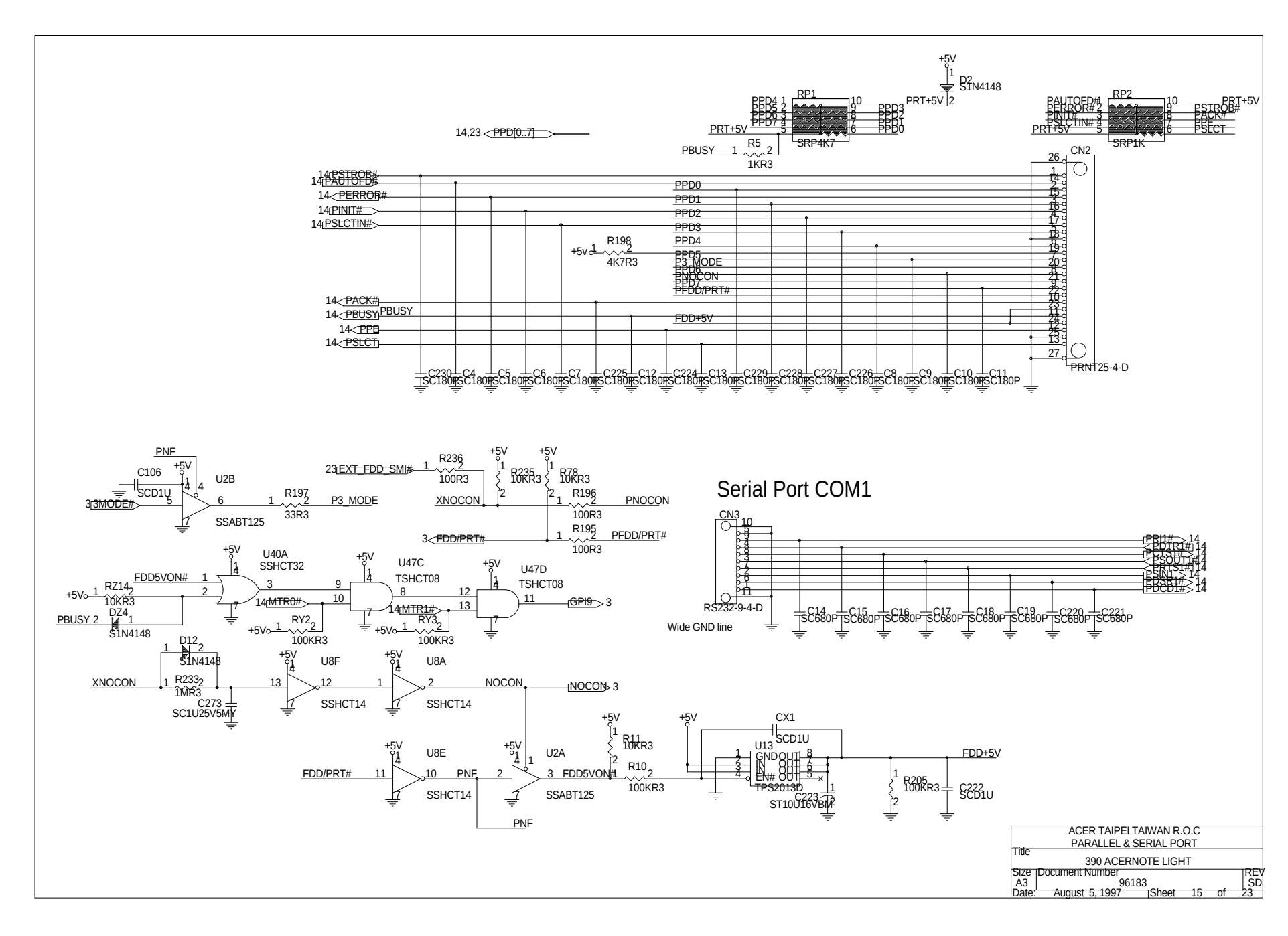

A_SLOT_VCC
B_SLOT_VCC
+3.3V
+5V
+12V
C127 SCD1U
C126 SCD1U
C119 SCD1U
C128 SC22U10V0ZY
C140 SCD1U
C139 SCD1U
C145 SCD1U
C321 ST22U
C138 SCD1U
C107 SCD1U
C302 SC2D2U50V
C117 SCD1U
C116 SCD1U
C118 SCD1U
C319 SCD1U
C306 ST10U16VBM
C305 ST10U16VBM
C297 SCD1U
C326 SCD1U
C295 SCD1U
C296 SCD1U
A_VPP
B_VPP
C122 SCD1U
C313 SCD1U
CN16
AMP-CONN152
U31
TPS2206
3.3V
5V
12V
RESET
RESET#
DATA
CLOCK
LATCH
NC
OC#
AVPP
AVCC
BVCC
BVPP
GND
$PCIRST#
$DATA
$CLOCK
$LATCH
U12
LM75CIMX-3
SDA
SCL
O.S.
GND
A0
A1
A2
$SMBDATA
$SMBCLK
SYS_COM
RX29
22KR3
C151 SCD1U
C144 SCD1U
C322 ST10U16VBM
C143 SCD1U
C323 ST10U16VBM
CX3 ST100U10VDM
C121 SCD1U
C304 ST10U16VBM
C120 SCD1U
C303 ST10U16VBM
CX4 ST100U10VDM
RP22
RP23
RP16
RP15
RP14
SRP10K
U9D
SSHCT08
CARD_IN#
ACER TAIPEI TAIWAN R.O.C
PCMCIA SOCKET & POWER CONTROLLER TPS2206
390 ACERNOTE LIGHT
Size A3
Document Number 96183
REV SD
Date: August 7, 1997
Sheet 12 of 23

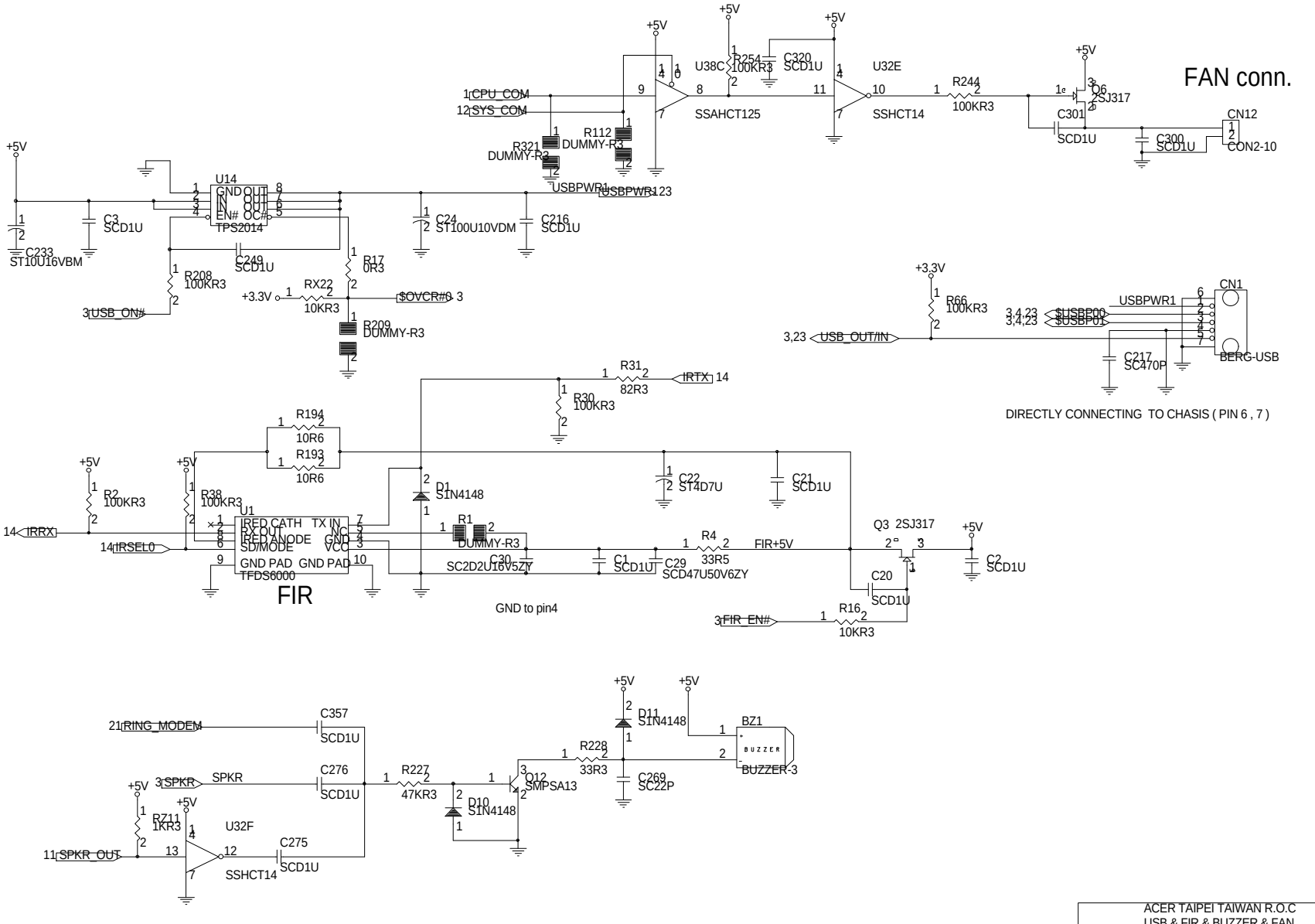


Touch Pad & Internal Keyboard

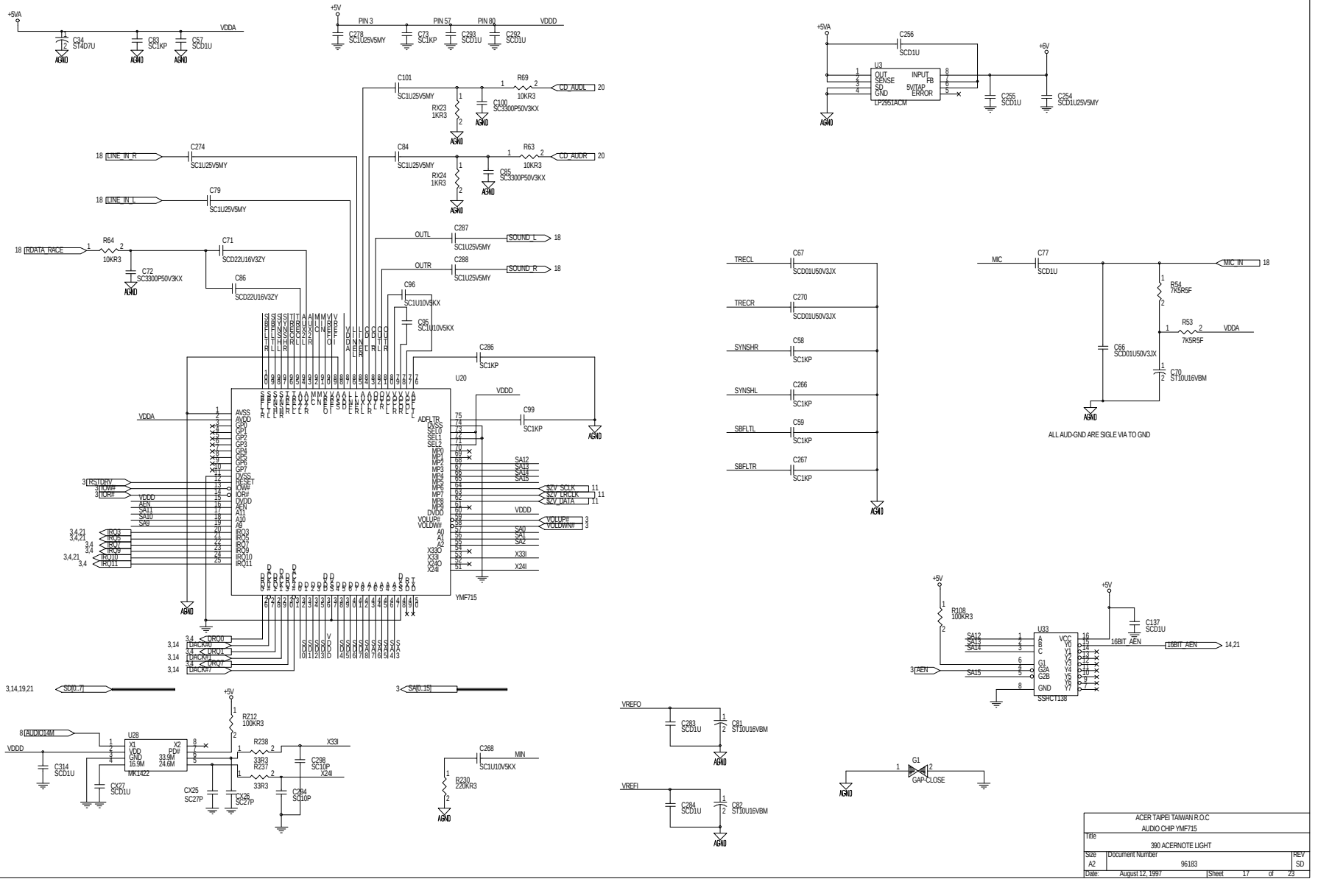
ACER TAIPEI TAIWAN R.O.C		
M38813 & LED & CHARGER SMBUS		
Title	390 ACERNOTE LIGHT	
Size A3	Document Number 96183	REV SD
Date: August 4, 1997	Sheet 13 of 23	


PLACE BYPASS CAPS COLSE TO IC'S
C27 SCD1U
C31 SCD1U
C44 SCD1U
C65 SCD1U
C52 SCD22U16V3ZY
C28 SCD22U16V3ZY
U17
FDC37C672-1
RN2
RN3
RN4
RN1
R6 33R3
R20 1KR3
SRN33
PPD[0..7]
SD[0..7]
SA[0..11]
DRQ[1..3]
INDEX#
TRK0#
WRTPRT#
RDATA#
DSKCHG#
CLOCKI
RESET_DRV
RSTDRV
DACK#[1..3]
TC
IRQ4
IRQ3
IOR#
IOW#
AEN
16BIT_AEN
IOCHRDY
IRRX
IRTX
RTS1#
DCD1#
SIN1
SOUT1
DSR1#
DTR1#
CTS1#
RI1#
INIT#
AUTOFD#
STROBE#
SLCTIN#
ERROR#
PE
BUSY
ACK#
SLCT
PSTROBE#
PACK#
PBUSY
PPE
PSLCT
PERROR#
PAUTOFD#
PSOUT1#
PDTR1#
PDSR1#
PDRI1#
PDCD1#
PCTS1#
PSIN1#
R56 10KR3
R58 10KR3
R51 10KR3
R41 10KR3
R34 10KR3
R33 100KR3
R27 0R3
RI_232#
U18
MAX3243
C46 SCD047U
C47 SCD33U16V3ZY
C80 SC1U10V5K
C253 SCD33U16V3ZY
C51 SCD33U16V3ZY
NOTE: 1.The IR transmission use the standard UART2
TXD2 and RXD2 pins, NOT IRTX and IRRX pins.
2.The IRQ's are IRQ3-7 and IRQ10-12.
3.The DACK#'s are DACK#1-3.
4.The DRQ's are DRQ1-3.
ACER TAIPEI TAIWAN R.O.C
SUPER I/O SMC672 & RS232 MAX3243
Title
390 ACERNOTE LIGHT
Size A3
Document Number 96183
REV SD
Date: August 12, 1997
Sheet 14 of 23

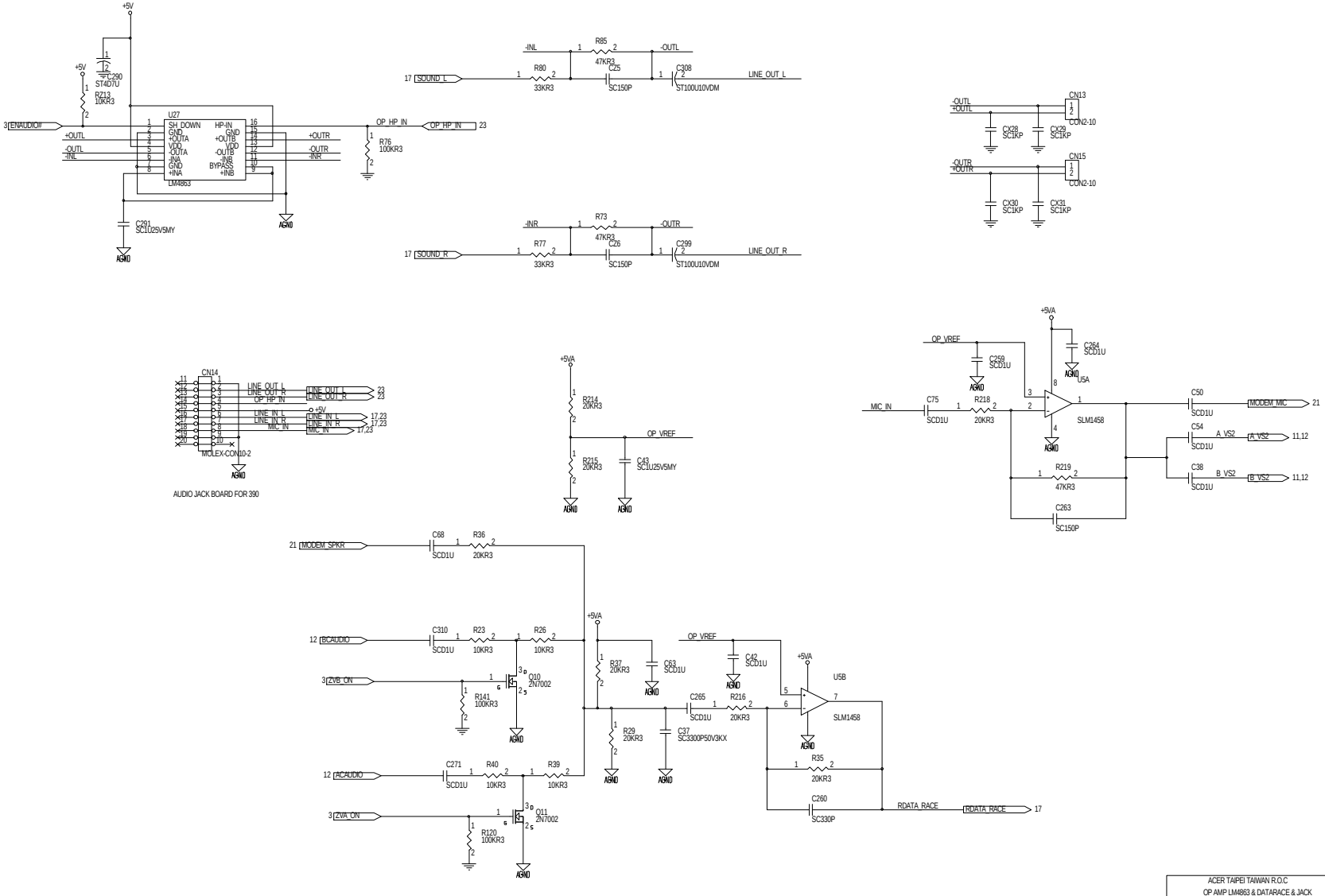

Serial Port COM1
ACER TAIPEI TAIWAN R.O.C
PARALLEL & SERIAL PORT
Title
390 ACERNOTE LIGHT
Size A3
Document Number 96183
REV SD
Date: August 5, 1997
Sheet 15 of 23



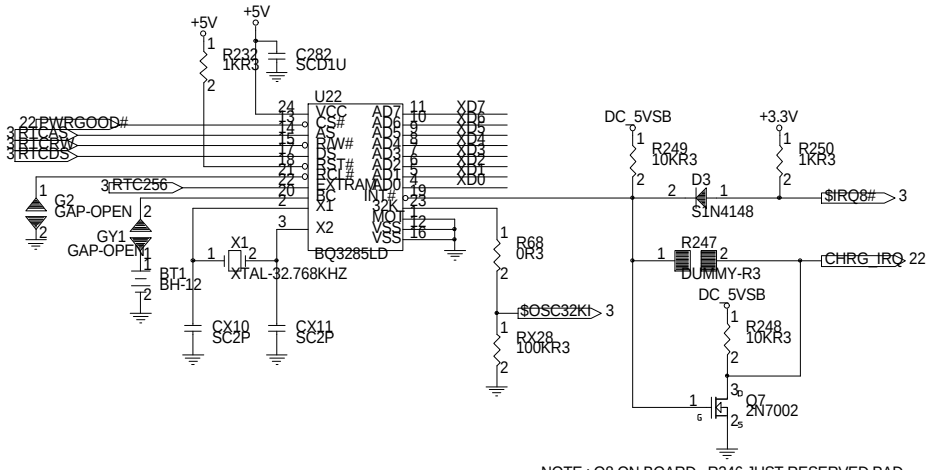
ACER TAIPEI TAIWAN R.O.C		
USB & FIR & BUZZER & FAN		
Title: 390 ACERNOTE LIGHT		
Size: A3	Document Number: 96183	REV: SD
Date: August 7, 1997	Sheet 16 of 23	



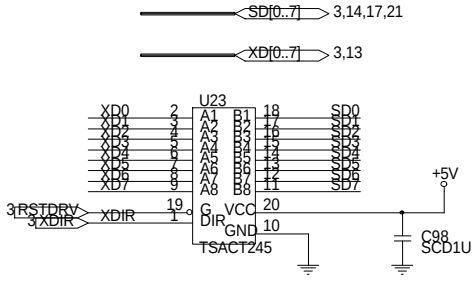
ACER TAIPEI TAIWAN R.O.C		
AUDIO CHIP YMF715		
Title	390 ACERNOTE LIGHT	
Size: A2	Document Number: 96183	REV: SD
Date: August 12, 1997	Sheet 17 of 23	

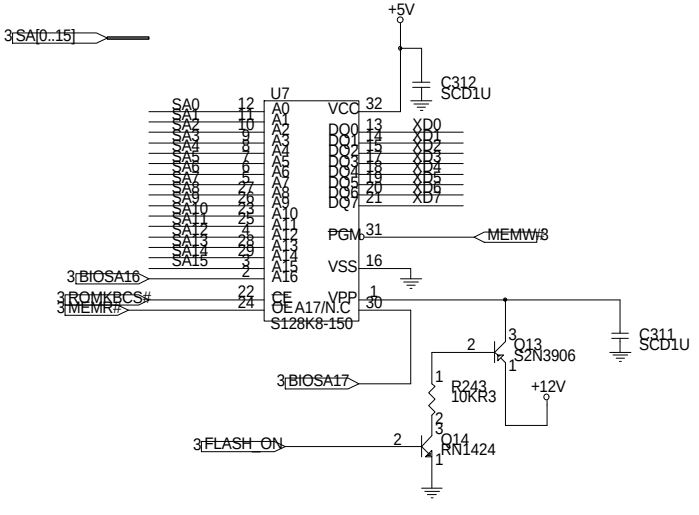


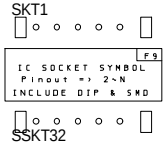
ACER TAIPEI TAIWAN R.O.C		
OP AMP LM4863 & DATARACE & JACK		
Title: 390 ACERNOTE LIGHT		
Size: A2	Document Number: 96183	REV: SD
Date: August 15, 1997	Sheet 18 of 23	



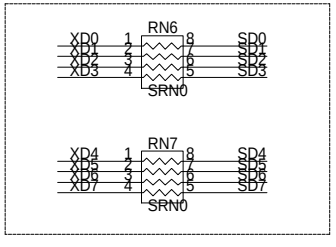
NOTE : Q8 ON BOARD , R346 JUST RESERVED PAD





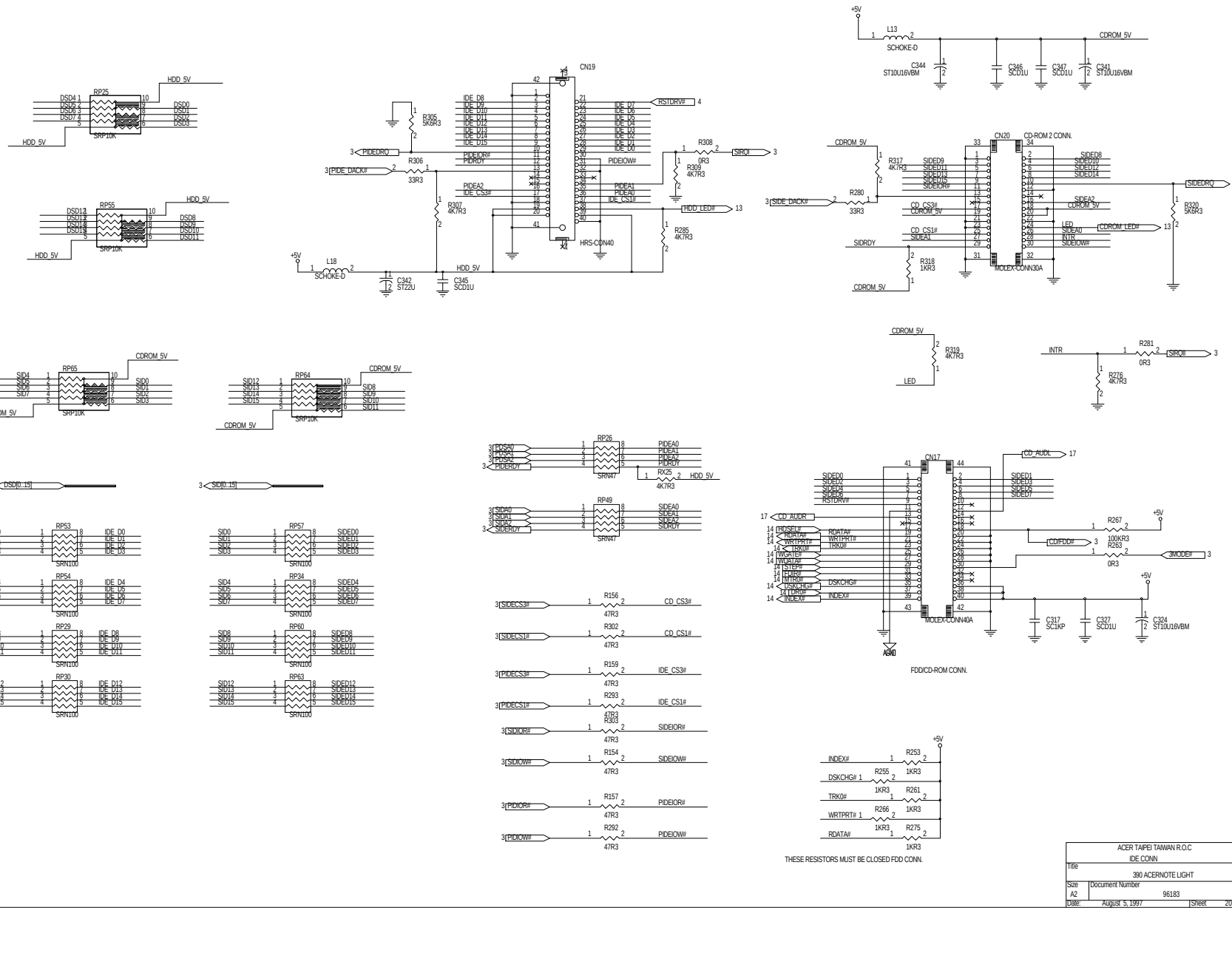


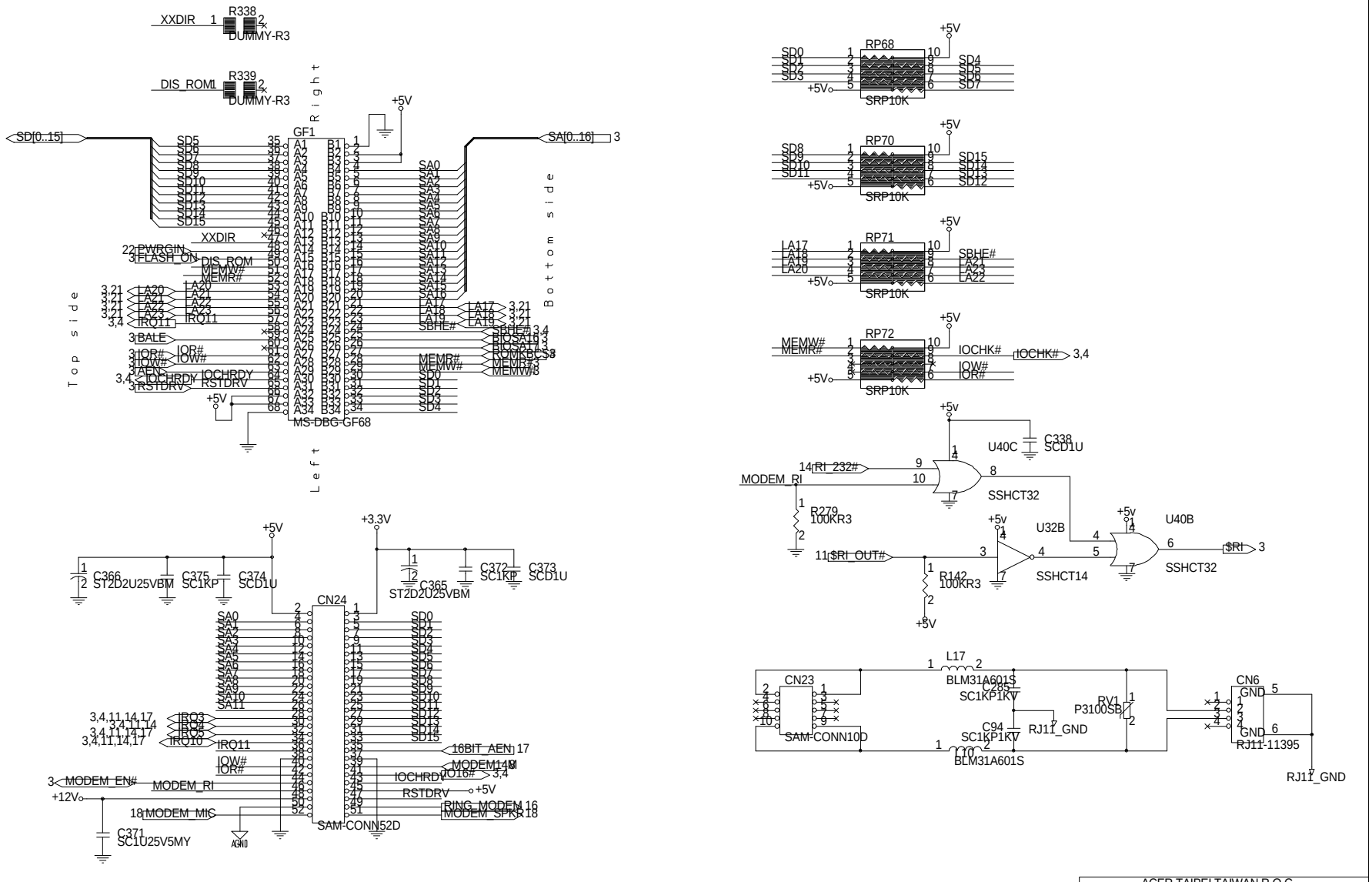
PLCC ROM SOCKET



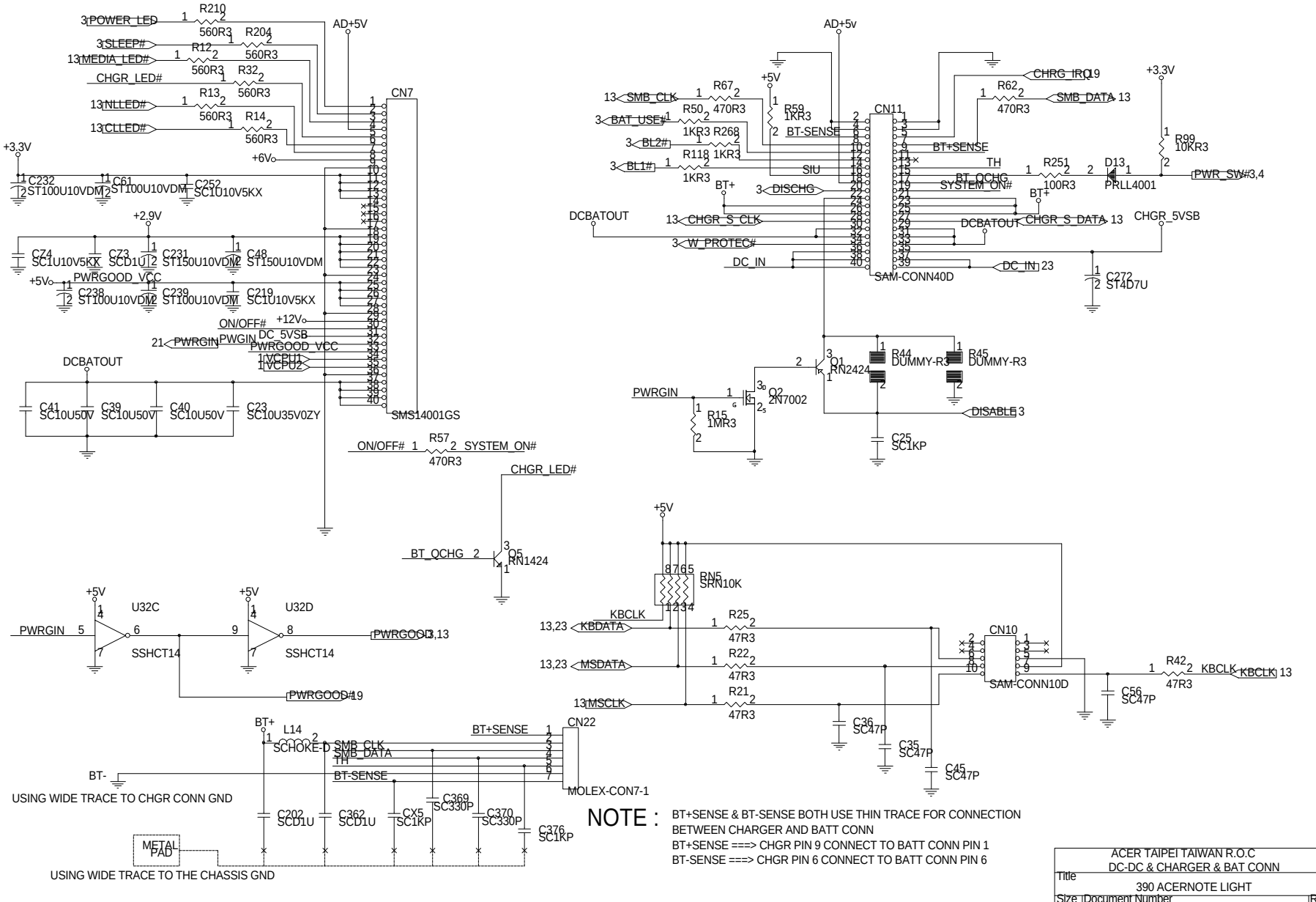
RESERVED
CONTROL FROM BOM

ACER TAIPEI TAIWAN R.O.C		
RTC & BIOS ROM		
Title	390 ACERNOTE LIGHT	
Size A3	Document Number 96183	REV SD
Date: August 21, 1997	Sheet 19 of 23	

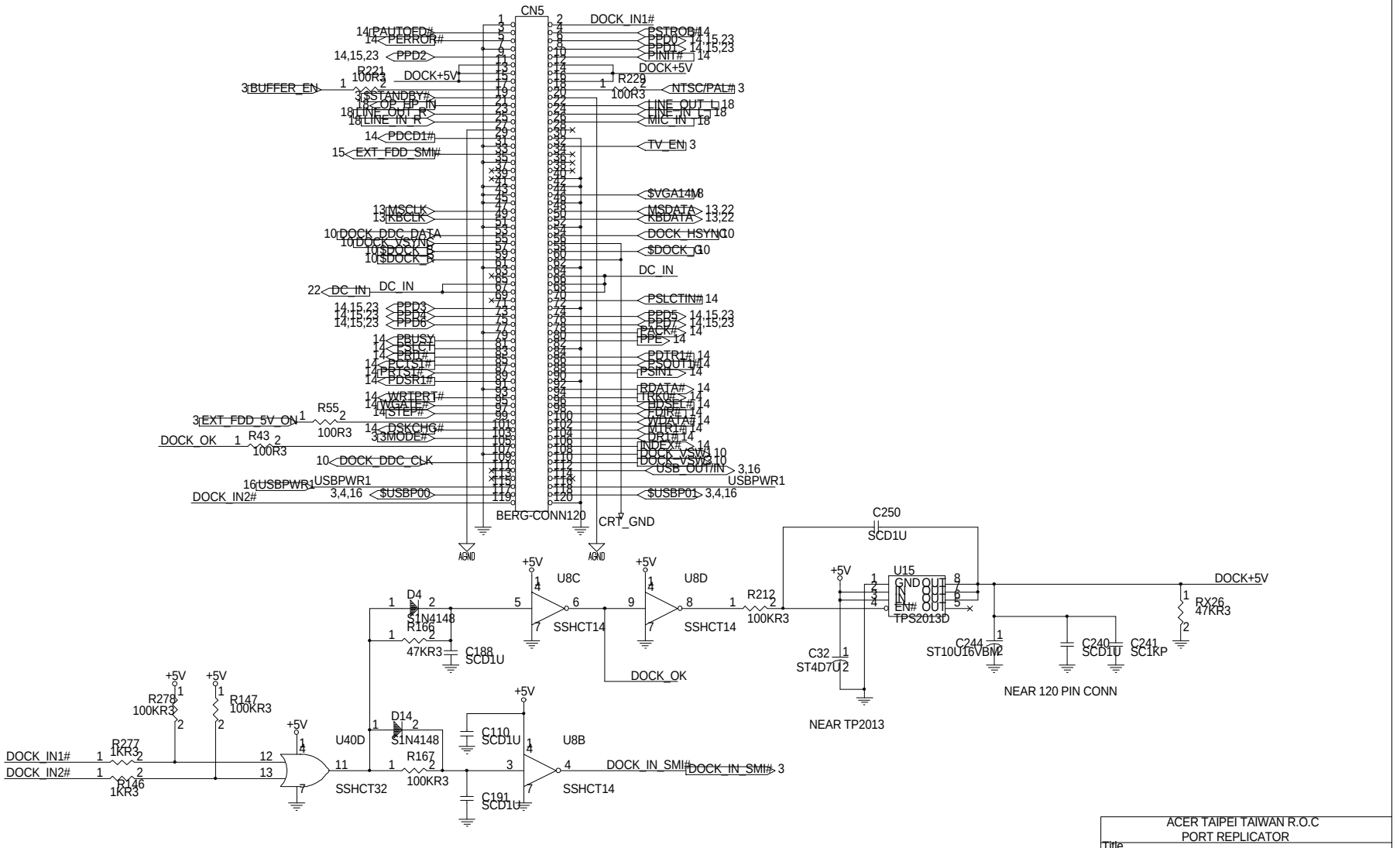

RP25
SRP10K
HDD_5V
DSD4 1
DSD5 2
DSD6 3
DSD7 4
DSD0
DSD1
DSD2
DSD3
RP55
DSD12
DSD13
DSD14
DSD15
DSD8
DSD9
DSD10
DSD11
CN19
HRS-CDN40
IDE_D8
IDE_D9
IDE_D10
IDE_D11
IDE_D12
IDE_D13
IDE_D14
IDE_D15
IDE_D7
IDE_D6
IDE_D5
IDE_D4
IDE_D3
IDE_D2
IDE_D1
IDE_D0
RSTDRV#
PIDEDRQ
PIDEIOR#
PIDRDY
PIDEIOW#
PIDEA2
IDE_CS3#
PIDEA1
PIDEA0
IDE_CS1#
PIDE_DACK#
R305 5K6R3
R306 33R3
R307 4K7R3
R308 0R3
R309 4K7R3
R285 4K7R3
SIRQI
HDD_LED#
L18
SCHOKE-D
C342 ST22U
C345 SCD1U
+5V
CDROM_5V
L13
C344 ST10U16VBM
C346 SCD1U
C347 SCD1U
C341 ST10U16VBM
CN20
CD-ROM 2 CONN.
MOLEX-CONN30A
R317 4K7R3
R280 33R3
R318 1KR3
R320 5K6R3
SIDED8
SIDED9
SIDED10
SIDED11
SIDED12
SIDED13
SIDED14
SIDED15
SIDEDRQ#
SIDEA2
CD_CS3#
CD_CS1#
SIDEA1
SIDEA0
INTB
SIDEIOW#
LED
CDROM_LED#
SIDE_DACK#
SIDRDY
SIDEDRQ
RP65
RP64
SRP10K
SID4
SID5
SID6
SID7
SID0
SID1
SID2
SID3
SID12
SID13
SID14
SID15
SID8
SID9
SID10
SID11
R319 4K7R3
LED
INTR
R291 0R3
SIRQII
R276 4K7R3
RP26
RP49
SRN47
PDSA0
PDSA1
PDSA2
PIDERDY
PIDEA0
PIDEA1
PIDEA2
PIDRDY
SIDA0
SIDA1
SIDA2
SIDERDY
SIDEA0
SIDEA1
SIDEA2
SIDERDY
RX25 4K7R3
HDD_5V
CN17
MOLEX-CONN40A
FDD/CD-ROM CONN.
CD_AUDL
CD_AUDR
HDSEL#
RDATA#
WRTPRT#
TRK0#
WGATE#
WDATA#
STEP#
FDIR#
INTRQ#
DSKCHG#
HDRQ#
INDEX#
SIDED0
SIDED1
SIDED2
SIDED3
SIDED4
SIDED5
SIDED6
SIDED7
RSTDRV#
R267 100KR3
CD/FDD#
R263 0R3
3MODE#
C317 SC1KP
C327 SCD1U
C324 ST10U16VBM
AGND
DSD[0..15]
SID[0..15]
RP53
RP54
RP29
RP30
RP57
RP34
RP60
RP63
SRN100
IDE_D0
IDE_D1
IDE_D2
IDE_D3
IDE_D4
IDE_D5
IDE_D6
IDE_D7
IDE_D8
IDE_D9
IDE_D10
IDE_D11
IDE_D12
IDE_D13
IDE_D14
IDE_D15
SIDED0
SIDED1
SIDED2
SIDED3
SIDED4
SIDED5
SIDED6
SIDED7
SIDED8
SIDED9
SIDED10
SIDED11
SIDED12
SIDED13
SIDED14
SIDED15
R156 47R3
R302 47R3
R159 47R3
R293 47R3
R303 47R3
R154 47R3
R157 47R3
R292 47R3
SIDECS3#
SIDECS1#
PIDECS3#
PIDECS1#
SIDIOR#
SIDIOW#
PIDIOR#
PIDIOW#
CD_CS3#
CD_CS1#
IDE_CS3#
IDE_CS1#
SIDEIOR#
SIDEIOW#
PIDEIOR#
PIDEIOW#
R253 1KR3
R255 1KR3
R261 1KR3
R266 1KR3
R275 1KR3
INDEX#
DSKCHG#
TRK0#
WRTPRT#
RDATA#
THESE RESISTORS MUST BE CLOSED FDD CONN.
ACER TAIPEI TAIWAN R.O.C.
IDE CONN.
Title
390 ACERNOTE LIGHT
Size
A2
Document Number
96183
REV
SD
Date: August 5, 1997
Sheet 20 of 23



ACER TAIPEI TAIWAN R.O.C		
GOLDEN FINGER & MODEM CONN		
Title	390 ACERNOTE LIGHT	
Size: A3	Document Number: 96183	REV: SD
Date: August 5, 1997	Sheet 21 of 23	



ACER TAIPEI TAIWAN R.O.C		
DC-DC & CHARGER & BAT CONN		
Title	390 ACERNOTE LIGHT	
Size A3	Document Number 96183	REV SD
Date: August 14, 1997	Sheet 22 of 23	


CN5
BERG-CONN120
CRT_GND
DOCK_IN1#
DOCK_IN2#
DOCK+5V
DC_IN
BUFFER_EN
EXT_FDD_5V_ON
DOCK_OK
USBPWR1
DOCK_IN_SMI#
TV_EN
LINE_OUT_L
LINE_OUT_R
LINE_IN_L
LINE_IN_R
MIC_IN
NTSC/PAL#
DOCK_DDC_DATA
DOCK_DDC_CLK
DOCK_VSYNC
DOCK_HSYNC
USB_OUT/IN
U8C
U8D
U40D
U8B
U15
SSHCT14
SSHCT32
TPS2013D
S1N4148
NEAR TP2013
NEAR 120 PIN CONN
ACER TAIPEI TAIWAN R.O.C
PORT REPLICATOR
390 ACERNOTE LIGHT
Size A3
Document Number 96183
REV SD
Date: August 5, 1997
Sheet 23 of 23

BIOS POST Checkpoints

This appendix lists the POST checkpoints of the notebook BIOS.

Table E-1 POST Checkpoint List

Checkpoint	Description
04h	• Dispatch Shutdown Path ***Note:*** *At the beginning of POST, port 64 bit 2 (8042 system flag) is read to determine whether this POST is caused by a cold or warm boot. If it is a cold boot, a complete POST is performed. If it is a warm boot, the chip initialization and memory test is eliminated from the POST routine.*
08h	• Reset PIE, AIE, UIE ***Note:*** *These interrupts are disabled in order to avoid any incorrect actions from happening during the POST routine.*
09h	• Initialize m1531
0Ah	• Initialize m1533 • Initialize m7101
10h	• DMA(8237) testing & initialization
14h	• System Timer(8254) testing & initialization
18h	• DRAM refresh cycle testing • Set default SS:SP= 0:400
1Ch	• CMOS shutdown byte test, battery, and check sum ***Note:*** *Several parts of the POST routine require the system to be in protected mode. When returning to real mode from protected mode, the processor is reset, therefore POST is re-entered. In order to prevent re-initialization of the system, POST reads the shutdown code stored in location 0Fh in CMOS RAM. Then it jumps around the initialization procedure to the appropriate entry point.* *The CMOS shutdown byte verification assures that CMOS 0Fh area is fine to execute POST properly.* • Initialize default CMOS setting if CMOS bad • Initialize RTC time base ***Note:*** *The RTC has an embedded oscillator that generates a 32.768 KHz frequency. To initialize the RTC time base, turn on this oscillator and set a divisor to 32768 so that the RTC can count time correctly*
1Dh, 1Eh	• DRAM type determination
2Ch	• 128K base memory testing • Set default SS:SP= 0:400 ***Note:*** *The 128K base memory area is tested for POST execution. The remaining memory area is tested later.*

Table E-1 POST Checkpoint List

Checkpoint	Description
20h	• KB controller(8041/8042) testing • KB type determination • Write default command byte upon KB type
24h	• PIC(8259) testing & initialization
30h	• System Shadow RAM
34h	• DRAM sizing
3Ch	• Initialize interrupt vectors
4Bh	• Identify CPU brand and type
35h	• PCI pass 0
40h	• Assign I/O if device request
41h	• Assign Memory if device requested
44h	• Assign IRQ if device request
45h	• Enable command byte if device is OK
50h	• Initialize Video display
52h	• Download keyboard matrix
4Ch	• ChipUp initialization for CPU clock checking
54h	• Process VGA shadow region
58h	• Set POST screen mode(Graphic or Text) • Display Acer(or OEM) logo if necessary • Display Acer copyright message if necessary • Display BIOS serial number
59h	• Hook int vector 1ch for POST quiet boot
5Ch	• Memory testing
5Ah	• SMRAM test and SMI handler initialization
4Eh	• Audio initialization
60h	• External Cache sizing • External Cache testing(SRAM & Controller) • Enable internal cache if necessary • Enable external cache if necessary
64h	• Reset KB device • Check KB status ***Note:*** *The keyboard LEDs should flash once.*
7Ch	• Reset pointing device • Check pointing device
70h	• Parallel port testing
74h	• Serial port testing
78h	• Math Coprocessor testing

Table E-1 POST Checkpoint List

Checkpoint	Description
80h	• Set security status
84h	• KB device initialization • Enable KB device
6Ch	• FDD testing & parameter table setup ***Note:*** *The FDD LED should flash once and its head should be positioned*
88h	• HDD testing & parameter table setup
89h	• Get CPU MUX ***Note:*** *This routine is to identify the user-set CPU frequency, not CPU-required frequency*
90h	• Display POST status if necessary
93h	• Rehook int1c for quiet boot
94h	• Initialize I/O ROM
A4h	• Initialize security feature
A8h	• Setup SMI parameters
A0h	• Initialize Timer counter for DOS use
ACh	• Enable NMI • Enable parity checking • Set video mode
B0h	• Power-on password checking • Display configuration table • Clear memory buffer used for POST • Select boot device